

RT Box controlCARD Interface

User Manual September 2019

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RT Box controlCARD Interface

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Introduction

The PLECS RT Box is a powerful real-time simulator based on a 1 GHz Xilinx Zynq system on a chip (SOC). With its 64 digital and 32 analog I/O signals, the RT Box is well equipped for hardware-in-the-loop (HIL) testing as well as rapid control prototyping.

If employed for HIL testing, the RT Box typically emulates the power stage of a power electronic system. The power stage could be a simple DC/DC converter, an AC drive system or a complex multi-level inverter system. The device under test (DUT) is the control hardware connected to the RT Box. In such a setup, the complete controller can be tested without the real power stage.

To simplify the connection of external hardware and to provide convenient access to the RT Box inputs and outputs, Plexim offers a set of RT Box accessories.

The **controlCARD Interface** described in this document has two control-CARD slots which facilitate a simple connection of the RT Box with the 100pin and 180-pin controlCARD modules from Texas Instruments (TI). It enables users to test control algorithms implemented on C2000 MCUs without developing their own interface hardware. The pinout of the controlCARD Interface board has been optimized for the following development kits:

- Piccolo controlCARDs (280049, 28027, 28035, 28075)
- Delfino controlCARDs (28335, 2837xD)
- Concerto controlCARDs (F28M35, F28M36)

The controlCARD Interface may also be used with other development boards compliant with the controlCARD pinout.

Interface Board Overview

The interface board provides a 100-pin socket for the older 100-pin control-CARDs, as well as a 180-pin socket for the newer modules. Fig. 2.1 shows the top view of the controlCARD interface board.

All RT Box output signals are buffered to protect the MCU from overvoltage, and local opamps provide a low-impedance source for the MCUs ADC inputs. The board provides access to three analog outputs labeled *AOUT-13...15* via BNC connectors. For status communication with the RT Box, the board features four sliding switches and four LEDs labeled *DIO-28...DIO-31*.

Additionally, external JTAG adapters can be connected to the MCUs by means of two 14-pin headers labeled *JTAG-100*, *JTAG-180*. Each controlCARD is wired to an isolated CAN driver, allowing communication among the control-CARDs as well as external equipment. The board also provides a 64 kbit Serial Electrically Erasable PROM for user specific purposes.

A 6-pin unshrouded connector labeled *SCI* for FTDI cable is provided to communicate with older 100-pin controlCARDs which do not support serial interface.

ControlCARD Socket Pins

Tables 2.1 and 2.2 list the pin assignments of 100-pin and 180-pin control-CARD sockets and the RT Box signals.

A more detailed table, including the available processor functions at each pin for the supported controlCARDs, can be found in the Appendix.

RT Box	100-pin		RT Box
	1	51	
	2	52	
	3	53	
	4	54	
	5	55	
	6	56	
AO14	7	57	AO15
	8	58	
AO12	9	59	AO13
	10	60	
AO10	11	61	A011
	12	62	
AO8	13	63	AO9
	14	64	
AO6	15	65	AO7
	16	66	
A04	17	67	AO5
	18	68	
AO2	19	69	AO3
	20	70	
AO0	21	71	AO1
	22	72	
DI17	23	73	DI16
DI19	24	74	DI18
DI21	25	75	DI20

RT Box	100)-pin	RT Box
DI23	26	76	DI22
	27	77	
DI25	28	78	DI24
DI27	29	79	DI26
DI29	30	80	DI28
	31	81	
	32	82	
	33	83	DO0
	34	84	DO5
DO6	35	85	DO7
DO4	36	86	
	37	87	
	38	88	
	39	89	
DO2	40	90	DO3
	41	91	DO1
	42	92	
	43	93	
	44	94	
DI31	45	95	DI30
	46	96	
	47	97	
	48	98	
	49	99	
	50	100	

Table 2.1: 100-pin controlCARD socket

56 $6970DO14787172DO24A0159107374DO26A0131112A014DO257576A0131112A014DO247778A0111516DO237980A0111516DO228182$	RT Box	180)-pin	RT Box		RT Box	180)-pin	RT Box
56 $6-970DO14A0159107172DO22A0131112AO14DO257576A0131112AO14DO247778A0111516DO237980A091718AO10DO228182A091718AO10DO228182A091718AO10DO228182A032324AO68788D114A032526AO4DO218990D115A012728AO2D020919291NC3346NC97989691D104950D14101102D019D135556D17107108109100D135556D17107108119120D106162D011121122122122$		1	2		· -		65	66	
78778AO159107172DO27AO159107374DO26AO131112AO14DO2575761314AO12DO247778AO111516DO237980AO91718AO10DO228182AO91718AO10DO228182AO721228586100AO32526AO4DO218990D113AO12728AO2DO209192100AO12728AO29596100NC3346NC9798100101DI04950DI4101102D014DI15152DI5103104D017DI25354DI6105106D016DI35556DI7107108119120DI106162D011121122121122		3	4		· -		67	68	DO13
AO159107374DO26AO131112AO14DO257576DO261314AO12DO247778DO237980AO111516DO237980DO237980AO91718AO10DO228182DO237980AO91718AO10DO228182DO237980DO23AO72122DO237980DO247778AO52324AO68384DO247788D114AO32526AO4DO218990D115AO12728AO2D0209192D15D0209192NC3346NC9798D019D019D019D019DI04950DI4101102D018D019DI35556DI7107108D110D110D12DI35758D112NC109118NCDI95960D113119120RESET (TD1106162D011121122D12		5	6		· -		69	70	DO14
AO131112AO141314AO12AO111516AO91718AO10 $AO9$ 1718AO101920AO8AO72122AO52324AO6AO32526AO4AO12728AO22930AO0313295NC3346NC474899DI04950DI15152DI35556DI7107108DI95960DI106162DI106162		7	8		· -		71	72	DO27
1314AO12AO111516AO91718AO10 $AO9$ 1718AO101920AO8AO72122AO52324AO6AO32526AO4AO12728AO2AO12728AO2AO12728AO2AO12728AO2AO13132AO13132AO150DI4DI04950DI4DI15152DI5DI35556DI7DI35758DI12DI106162DO11	AO15	9	10		-		73	74	DO26
AO111516DO237980AO91718AO10DO228182AO91718AO10DO228182AO72122 $3384344AO52324AO68788DI14AO32526AO4DO218990DI15AO12728AO2DO209192304AO12728AO2DO209192304AO12728AO29596314AO13132959631432NC3346NC9798314DI04950DI4101102DO16DI15152DI5103104DO16DI35556DI7107108314DI95960DI13119120RESET (IDI106162DO11121122312$	AO13	11	12	A014		DO25	75	76	
AO91718AO101920AO8AO72122AO52324AO6AO32526AO4AO12728AO2D0209192Construction2930AO031329596NC3346NCDI04950DI4DI15152DI5DI35556DI7DI85758DI12DI106162DO11		13	14	AO12	-	DO24	77	78	
1920A08A072122	AO11	15	16			DO23	79	80	
AO72122 $\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	AO9	17	18	AO10	-	DO22	81	82	
AO5 23 24 AO6 AO3 25 26 AO4 D021 89 90 D114 AO1 27 28 AO2 D020 91 92 92 AO1 27 28 AO2 D020 91 92 92 AO1 27 28 AO2 D020 91 92 92 AO1 31 32 D020 91 92 93 94 94 NC 3346 NC 95 96 96 91 92 NC 3346 NC 97 98 99 100 D019 DI0 47 48 D16 97 98 90 9019 DI1 51 52 D15 103 104 D017 DI3 55 56 D17 107 108 NC D19 59 60 D113 119 120 <i>RESET</i> (D D110 61 62 D011 121 122		19	20	AO8	-		83	84	
AO3 25 26 AO4 AO1 27 28 AO2 D021 89 90 DI15 D020 91 92 92 D021 93 94 94 D020 91 92 94 D020 91 92 94 D10 31 32 95 96 NC 3346 NC 97 98 99 D10 47 48 99 100 D019 D10 49 50 D14 101 102 D018 D11 51 52 D15 103 104 D017 D12 53 54 D16 105 106 D016 D13 55 56 D17 NC 109118 NC D19 59 60 D113 119 120 RESET (D17) D10 61 62 D011 121 122 121	AO7	21	22		· -		85	86	
AO1 27 28 AO2 29 30 AO0 D020 91 92 31 32 93 94 93 94 NC 3346 NC 95 96 97 98 NC 3746 NC 97 98 99 100 D019 DI0 49 50 DI4 99 100 D019 DI1 51 52 DI5 103 104 D017 DI2 53 54 DI6 105 106 D016 DI3 55 56 DI7 NC 107118 NC DI8 57 58 DI12 NC 119 120 <i>RESET</i> (I DI10 61 62 D011 121 122 121 122	AO5	23	24	AO6	-		87	88	DI14
29 30 AOO 93 94 94 31 32 95 96 96 NC 3346 NC 97 98 99 A7 48 99 100 DO19 DI0 49 50 DI4 101 102 DO18 DI1 51 52 DI5 103 104 DO16 DI2 53 54 DI6 105 106 DO16 DI3 55 56 DI7 107 108 NC DI9 59 60 DI13 NC 119 120 RESET (D DI10 61 62 DO11 121 122 124	AO3	25	26	AO4	· -	DO21	89	90	DI15
31 32 95 96 NC 3346 NC 97 98 47 48 99 100 DO19 DI0 49 50 DI4 101 102 DO18 DI1 51 52 DI5 103 104 DO16 DI2 53 54 DI6 105 106 DO16 DI3 55 56 DI7 107 108 DO16 DI8 57 58 DI12 NC 109118 NC DI9 59 60 DI13 119 120 RESET (D DI10 61 62 DO11 121 122 121	A01	27	28	AO2	· -	DO20	91	92	
NC 3346 NC 97 98 47 48 99 100 $D018$ DI0 49 50 $DI4$ 101 102 $D018$ DI1 51 52 $DI5$ 103 104 $D016$ DI2 53 54 $DI6$ 105 106 $D016$ DI3 55 56 $DI7$ 107 108 $D16$ DI8 57 58 $DI12$ NC 107118 NC DI9 59 60 $D113$ 119 120 $RESET (D)$ DI10 61 62 $D011$ 121 122 121		29	30	AO0	· -		93	94	
47 48 99 100 D019 DI0 49 50 DI4 101 102 D018 DI1 51 52 DI5 103 104 D019 DI2 53 54 DI6 105 106 D016 DI3 55 56 DI7 107 108 D016 DI8 57 58 DI12 NC 109118 NC DI9 59 60 DI13 119 120 RESET (19) DI10 61 62 DO11 121 122 121		31	32				95	96	
DI0 49 50 DI4 DI1 51 52 DI5 DI2 53 54 DI6 DI3 55 56 DI7 DI8 57 58 DI12 DI9 59 60 DI13 DI10 61 62 DO11	NC	33.	46	NC			97	98	
DI1 51 52 DI5 DI2 53 54 DI6 103 104 DO17 DI3 55 56 DI7 105 106 DO16 DI3 55 56 DI7 107 108 DO16 DI8 57 58 DI12 NC 109118 NC DI9 59 60 DI13 119 120 RESET (II) DI10 61 62 DO11 121 122		47	48		-		99	100	DO19
DI2 53 54 DI6 105 106 D016 DI3 55 56 DI7 107 108 D016 DI8 57 58 DI12 NC 107 108 NC DI9 59 60 DI13 119 120 RESET (19) DI10 61 62 DO11 121 122 101	DI0	49	50	DI4	-		101	102	DO18
DI3 55 56 DI7 DI8 57 58 DI12 NC 107 108 DI9 59 60 DI13 NC 109118 NC DI10 61 62 DO11 121 122	DI1	51	52	DI5	· -		103	104	DO17
DI8 57 58 DI12 DI9 59 60 DI13 DI10 61 62 DO11	DI2	53	54	DI6	· -		105	106	DO16
DI9 59 60 DI13 DI10 61 62 DO11 119 120 RESET (I	DI3	55	56	DI7	· -		107	108	
DI10 61 62 DO11 121 122	DI8	57	58	DI12	· -	NC	109.	118	NC
	DI9	59	60	DI13	· -		119	120	RESET (I
DI11 63 64 DO12 NC 123180 NC	DI10	61	62	DO11			121	122	
	DI11	63	64	DO12	· -	NC	123.	180	NC

Table 2.2: 180-pin controlCARD socket

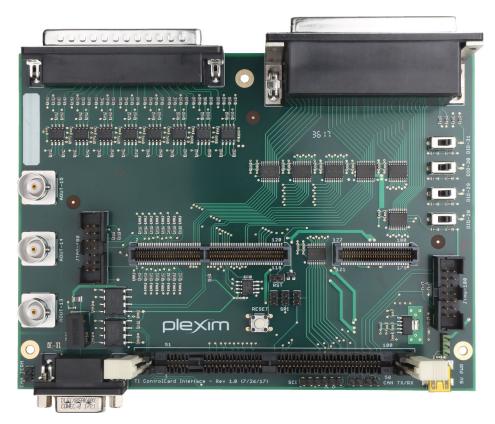


Figure 2.1: RT Box controlCARD Interface Board

Onboard Voltage Supply

Power to the controlCARD interface board can be supplied in two ways, by selecting the appropriate jumper terminals on the bottom right corner of the board. One way is to supply power directly from the RT Box. The second is through an external source using the USB connector labeled 5V PWR. This allows the board to be used without the RT Box. The interface board contains a linear voltage regulator that steps down the 5V supplied externally or by the RT Box to 3.3V required by the controlCARD. A green LED on the lower right section of the board indicates power supply to the board.

Analog Output

All 16 analog outputs from the RT Box are routed to both 100-pin and 180pin control card slots. It is possible to operate two cards at the same time, although the user must be aware that the sampling of one MCU could affect the measurements of the other. If both control card slots are populated, the analog signals must be shared by the controlCARDs. Three analog output channels *AOUT*-13...*AOOUT*-15 are also accessible at the BNC connectors.

All 16 analog output signals are passed through a rail-to-rail CMOS operational amplifier signal conditioning circuit, as shown in Fig. 2.2, for scaling the voltages to 0V and 3.3V, and for protecting the inputs of the MCU from damage by over-voltage. This introduces a gain of 4.42/6.8 (or 0.65) in between the analog output pins of the RT Box and the analog input pins of the controlCARD.

Additionally, each analog channel routed to the 180-pin controlCARD socket is buffered with a capacitor (2200 pF) against ground, to lower the source impedance of the channel so that the sample and hold capacitor of the MCU can be charged quickly. A small resistance (56 Ω) is also placed in series to stabilize the driving opamp circuit.

The 100-pin controlCARD socket is excluded from this step and receives analog output signals directly after signal conditioning, as these resistors and capacitors are already populated on the 100-pin controlCARDS.

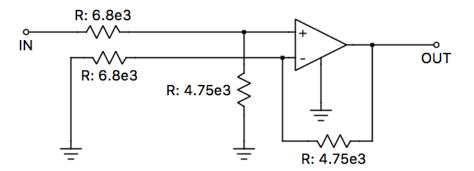


Figure 2.2: Analog Output Signal Conditioning Circuit

Digital I/O

Digital inputs DI0...DI15 from the RT Box are connected to the 180-pin controlCARD socket. DI16...DI31 are connected to the 100-pin controlCARD socket. Digital inputs DI28...31 can also be set via four sliding switches provided on the board labeled *DIO-28...DIO-31*.

Digital outputs DO0...DO7 are connected to the 100-pin controlCARD socket. DO11...DO14, DO16...27 are connected to the 180-pin controlCARD socket. DO28...DO31 are connected to four LEDs in the upper right section of the board labeled *DIO-28...DIO-31*.

All the digital input and output signals are buffered through bus transceivers to protect the inputs of the MCU from voltages greater than 3.3 V.

DO15 is connected to the 180-pin controlCARDs MCU reset pin via \overline{RST} jumper. If the jumper is set a low-level output at DO15 will reset the MCU. Do not set this jumper unless you wish to use this feature. Alternatively, the MCU can be reset using the push button labeled *RESET*.

CAN Communication

Two electrically isolated CAN transceivers provide CAN communication that can be accessed through a 9-pin D-SUB connector on the bottom left corner of the board. This allows communication among the controlCARDs, if populated together, as well as with external equipment.

Table 2.3 lists the pin assignments of the 9-pin D-SUB connector, 100-pin controlCARD and 180-pin controlCARD sockets.

Note CAN_L and CAN_H signals on pins 2 and 7 respectively on the 9-pin D-SUB connector can be terminated with a 120 Ω resistor using the jumper labeled *CAN TERM* located on the bottom left corner of the board.

JTAG Headers

Tables 2.4 and 2.5 list the pin assignments of JTAG headers for the 100-pin controlCARD labeled *JTAG-100* and 180-pin controlCARD labeled *JTAG-180*

100-pin	CAN Transceiver 1		9-pin connector	CAN Trar	180-pin	
			1			
94	TX1	CAN_L	2	CAN_L	TX2	82
		GND	3	GND		
			4			
			5			
		GND	6	GND		
44	RX1	CAN_H	7	CAN_H	RX2	80
			8			
			9			

Table 2.3: CAN pin assignment

respectively.

100-pin	Function	JTAG-100		Function	100-pin
49	TMS	1	2	TRST	99
97	TDI	3	4	GND	
	3 V	5	6	NC	
98	TDO	7	8	GND	
48	TCK	9	10	GND	
48	TCK	11	12	GND	
100	EMU0	13	14	EMU1	50

Table 2.4: JTAG-100 pin assignment

180-pin	Function	JTAG-180		Function	180-pin
3	TMS	1	2	TRST	4
8	TDI	3	4	GND	
	3 V	5	6	NC	
6	TDO	7	8	GND	
5	TCK	9	10	GND	
5	TCK	11	12	GND	
2	EMU0	13	14	EMU1	1

Table 2.5: JTAG-180 pin assignment

SCI Communication

Table 2.6 lists the pin assignments of the unshrouded connector labeled *SCI* for communication with older100-pin controlCARDs.

SCI	Function	100-pin
1 GND-		
2 NC		
3	VCC +	
4	TX <	43
5	RX >	93
6	NC	

Table 2.6: SCI pin assignment

3

Demo Application

On user's request, Plexim can provide the demo model listed below.

• Field Oriented Control of a PMSM

To be able to work with this model, the user would have to purchase a TI F28379D controlCARD.

Software Requirements

The PLECS model can be executed on Windows, MAC or Linux machines with the following software installed:

- PLECS Standalone (version 4.0.4 or higher)
- PLECS Standalone Coder

However, the control preprogrammed for the TI controlCARD can only be flashed or updated on a Windows machine (32-bit or 64-bit) with the following additional software installed:

• C2Prog – Download from www.codeskin.com (only required to reflash the MCU).

A license is required to run PLECS and use the code generation feature. You can request this license from Plexim at www.plexim.com.

Loading the Firmware

The following section shows how to program the MCU to flash the demo application or perform an update. Please note that this section is applicable for Windows machines only.

Populate the controlCARD on the 180-pin connector on the controlCARD interface board and switch on the RT Box. Connect the JTAG/SCI USB port of the controlCARD to your PC.

Open the Windows Device Manager and confirm that TI Debug Probes are listed.

You may have to install the FTDI drivers if the port is not enumerated.

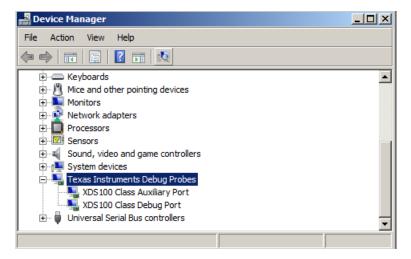


Figure 3.1: TI debug probes listed in device manager

The pre-compiled executable FOC_Controlcard_28379D_cpu01.ehx located in the demo package is used to begin. In C2Prog, select the file FOC_Controlcard_28379D_cpu01.ehx and configure the port to XDS100v2.

Click the **Program** button.

1

Figure 3.2: Flashing the controlCARD

Note The MCU can be reset using the push button labeled *RESET*.

Program the RT Box

This section describes the process of downloading a demo model to the RT Box. For general information about the RT Box and a manual on how to get started please also refer to the RT Box documentation available on the Plexim website at www.plexim.com.

Open the model FOC_controlcard180_hil.plecs located in the demo package. Familiarize yourself with the implementation of the subsystem PMSM and Inverter. Go to **Coder Options**. Select **PMSM and Inverter** and switch to the **Target** tab.

Coder Options: FOC_controlcard180_hil	2
System	General Parameter Inlining Target External Mode
FOC_controlcard180_hil	Target: PLECS RT Box 1
	Target device: rtbox-538.local.
	Analog input voltage range: -10 10 V
	Analog output voltage range: 0 5 V
	Digital output voltage level: 3.3 V
	Analog input sampling: Minimize latency
	Sampling delay (s): 0
	Enable external mode
	Overrun limit: 5
	Build
	Accept Revert Close Help

Figure 3.3: Programming the RT Box with the FOC Model

Select your **Target Device** from the drop-down list and click **Accept** and then **Build**. Your model is now compiled and downloaded to the RT Box automatically. Verify that the Blue **Running** LED on the RT Box is illuminated.

Connecting the External Mode

The External Mode enables access to the real-time simulation executed on the RT Box. It can be used to visualize all simulation signals via the model scopes.

Switch to the **External Mode** tab in the Coder Options and click **Connect** to start communication between PLECS and the model running on the RT Box. **Activate autotriggering** via the appropriate button.

Coder Options: FOC_controlcard180_hil	2
System	General Parameter Inlining Target External Mode
FOC_controlcard180_hil	Target device
	rtbox-538.local.
	Trigger controls
	Manual trigger
	Activate autotriggering Rate [Hz]: 20
	Trigger channel: 9; [Resolver/the]
	Sensitivity: Rising edge
	Trigger level: 0
	Trigger delay [steps]: 0
	Sampling
	Number of samples: 2048
	Decimation: 1
	Build
	Accept Revert Close Help

Figure 3.4: Connecting to the FOC Model via the External Mode

Flip Switch *DI29* to the left to enable the MCU drive control. Open the Scope **Scope** in the FOC model and analyze the control behavior.

RT Box Web Interface

The Web Interface provides information about the model running on the RT box as well as additional diagnostic options. It can be accessed by clicking on the \blacksquare icon under the *Target* or the *External Mode* tabs of the Coder Options dialog.

RT Box Web Interface: rtbox-538.local.	_ 🗆 🗵
PLECS RT Box 1	^
Application Frontipanel Rear panel Diagnostics Info	_
Model	
Model name: PMSM_and_Inverter Sample time: S µs	
Simulation	
Processor load:	
Current cycle time: 4.15 µs Maximum cycle time: 4.24 µs	
Reset Maximum	
Executable	
Browse	
Start automatically after upload Delay start until first scope trigger	
Start Stop	

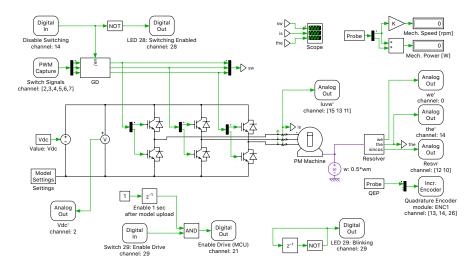
Figure 3.5: RT Box Web Interface

The processor load statistic reveals information about the time needed to calculate the model and therefore serves as a convenient tool to validate the chosen step size. Do not overload the processor and maintain a safety margin.

Note A model under actuation requires a higher processing time than an idle model. Additional processor load is required when using the external mode.

Description of Demo Projects

This section provides an overview of the FOC demo model and it's external signal availability.



Field Oriented Control of a PMSM

Figure 3.6: Field oriented control demo model

The project is based on a basic Field Oriented Control (FOC) application, with the embedded code controlling the switches of a three-phase inverter powering a permanent magnet (PM) machine.

The machine operates at Id= -200 A, Iq = 200 A, with a switching frequency of 20 kHz and a DC link voltage of 400 V.

The model outputs analog voltages for stator current measurements, the DC link voltage and the electrical angle (theta). The stator currents as well as theta can also be accessed directly via the BNC connectors. The rotor position and speed is made available using a quadrature encoder module via three digital outputs. The control algorithm generates six PWM signals controlling the inverter switches. Table 3.1 shows a detailed pin assignment for this demo model.

The speed of the motor can be changed in the PLECS model from 2500 rpm to 10000 rpm. At 10000 rpm, the motor is developing 50 kW.

A disable switching option in active high logic is implemented via DI14. LED 28 indicates if the switching signal is active. LED 29 blinks at a rate of 1 Hz while the model is running. Switch DI29 can be used to enable or disable the MCU drive. This information is forwarded to the MCU via DO21. Disconnect the \overline{RST} jumper and use the push button labeled *RESET* to reset the MCU.

Feature	RT Box Channel	180-pin Socket
	AO0	30
Vdc	AO2	28
Isa	AO15	9
Isb	AO13	11
Isc	AO11	15
$ heta_e$	AO14	12
	AO12	14
	AO10	18
ENC1A	DO13	68
ENC1B	DO14	70
ENC1I	DO26	74
PWM A H	DI2	53
PWM A L	DI3	55
PWM B H	DI4	50

PWM B L	DI5	52
PWM C H	DI6	54
PWM C L	DI7	56
Enable MCU	DO21	89
Disable PWM	DI14	88

Table 3.1: FOC I/O

Note Switch DI29 of the interface board enables or disables the MCU drive.

Appendix

Tables 4.1 and 4.2 provide more detailed information on the connectivity of the 180-pin controlCARD socket; table 4.3 provides more detailed information on the connectivity of the 100-pin controlCARD socket. For each controlCARD, the RT Box I/O is shown beside the controlCARD socket pins and the processor peripherals available at those pins.

TI F28379D ControlCard Pin Map

Function	RT Box	180)-pin	RT Box	Function
JTAG-EMU1		1	2		JTAG-EMU0
JTAG-TMS		3	4		JTAG-TRSTn
JTAG-TCK		5	6		JTAG-TDO
		7	8		JTAG-TDI
ADC-A0	AO15	9	10		
ADC-A1	AO13	11	12	AO14	ADC-B0
		13	14	AO12	ADC-B1
ADC-A2	A011	15	16		
ADC-A3	AO9	17	18	AO10	ADC-B2
		19	20	AO8	ADC-B3
ADC-A4	AO7	21	22		
ADC-A5	AO5	23	24	AO6	ADC-B4
ADCIN14	AO3	25	26	AO4	ADC-B5
ADCIN15	AO1	27	28	AO2	ADC-D0
		29	30	AO0	ADC-D1
	NC	31.	48	NC	
PWM1A, GPIO-00	DI0	49	50	DI4	PWM3A, GPIO-04
PWM1B, GPIO-01	DI1	51	52	DI5	PWM3B, GPIO-05
PWM2A, GPIO-02	DI2	53	54	DI6	PWM4A, GPIO-06
PWM2B, GPIO-03	DI3	55	56	DI7	PWM4B, GPIO-07
PWM5A, GPIO-08	DI8	57	58	DI12	PWM7A, GPIO-12
PWM5B, GPIO-09	DI9	59	60	DI13	PWM7B, GPIO-13
PWM6A, GPIO-10	DI10	61	62	DO11	PWM8A, GPIO-14
PWM6B, GPIO-11	DI11	63	64	DO12	PWM8B, GPIO-15

Function	RT Box	180)-pin	RT Box	Function
		65	66		
		67	68	DO13	QEP1A, GPIO-20
		69	70	DO14	QEP1B, GPIO-21
		71	72	DO27	QEP1S, GPIO-22
		73	74	DO26	QEP1I, GPIO-23
SPISIMOB, GPIO-24	DO25	75	76		
SPISOMIB, GPIO-25	DO24	77	78		
SPICLKB, GPIO-26	DO23	79	80		CANRXA
SPISTEB, GPIO-27	DO22	81	82		CANTXA
		83	84		
		85	86		
		87	88	DI14	GPIO-39
GPIO-40	DO21	89	90	DI15	GPIO-44
GPIO-41	DO20	91	92		
		93	94		
		95	96		
		97	98		
		99	100	DO19	QEP2A, GPIO-54
		101	102	DO18	QEP2B, GPIO-55
		103	104	DO17	QEP2S, GPIO-56
		105	106	DO16	QEP2I, GPIO-57
	NC	107.	118	NC	
		119	120	DO15	XRSn
	NC	121.	180	NC	

Table 4.1: TI 28379D ControlCard pin map

TI F280049M controlCARD Pin Map

Function	RT Box	180	180-pin RT Bo		Function
JTAG-EMU1		1	2		JTAG-EMU0
JTAG-TMS		3	4		JTAG-TRSTn
JTAG-TCK		5	6		JTAG-TDO
		7	8		JTAG-TDI
ADC-A0, B15, C15, DACA	AO15	9	10		
ADC-A1, DACB	AO13	11	12	A014	ADC-B0
		13	14	AO12	ADC-B1, A10, C10, PGA7_IN
ADC-A2, B6, PGA1_IN	A011	15	16		
ADC-A3	AO9	17	18	AO10	ADC-B2, C6, PGA3_IN
		19	20	AO8	ADC-B3, VDAC
ADC-A4, B8, PGA2_IN	AO7	21	22		
ADC-A5	AO5	23	24	AO6	ADC-B4, C8, C3, PGA4_IN
ADC-A6, PGA5_IN	AO3	25	26	AO4	ADC-C0
ADC-A9	AO1	27	28	AO2	ADC-C1
		29	30	AO0	ADC-C2
	NC	31.	48	NC	
PWM1A, GPIO-00	DI0	49	50	DI4	PWM3A, GPIO-04
PWM1B, GPIO-01	DI1	51	52	DI5	PWM3B, GPIO-05
PWM2A, GPIO-02	DI2	53	54	DI6	PWM4A, GPIO-06
PWM2B, GPIO-03	DI3	55	56	DI7	PWM4B, GPIO-07
PWM7A, GPIO-12	DI8	57	58	DI12	PWM5A, GPIO-08
PWM7B, GPIO-13	DI9	59	60	DI13	PWM6A, GPIO-10
PWM8A, GPIO-14	DI10	61	62	DO11	GPIO-39
PWM8B, GPIO-15	DI11	63	64	DO12	GPIO-23

Function	RT Box	180)-pin	RT Box	Function
		65	66		
		67	68	DO13	QEP1A, GPIO-40
		69	70	DO14	QEP1B, GPIO-57
		71	72	DO27	QEP1S, GPIO-22
		73	74	DO26	QEP1I, GPIO-31
SPISIMOB, GPIO-24	DO25	75	76		
SPISOMIB, GPIO-25	DO24	77	78		
SPICLKB, GPIO-26	DO23	79	80		CANRXA
SPISTEB, GPIO-27	DO22	81	82		CANTXA
		83	84		
		85	86		
		87	88	DI14	NC
GPIO-18	DO21	89	90	DI15	NC
NC	DO20	91	92		
		93	94		
		95	96		
		97	98		
		99	100	DO19	QEP2A, GPIO-24
		101	102	DO18	QEP2B, GPIO-25
		103	104	DO17	NC
		105	106	DO16	NC
	NC	107.	118	NC	
		119	120	DO15	XRSn
	NC	121.	180	NC	

Table 4.2: TI F280049M controlCARD pin map

TI F28335 controlCARD Pin Map

Function V33D-ISO	RT Box	100	D-pin	RT Box	Function
		1	51		V33D-ISO
		2	52		
		3	53		
		4	54		
		5	55		
GND-ISO		6	56		GND-ISO
ADCIN-B0	A014	7	57	AO15	ADCIN-A0
GND		8	58		GND
ADCIN-B1	AO12	9	59	AO13	ADCIN-A1
GND		10	60		GND
ADCIN-B2	AO10	11	61	AO11	ADCIN-A2
GND		12	62		GND
ADCIN-B3	AO8	13	63	AO9	ADCIN-A3
GND		14	64		GND
ADCIN-B4	AO6	15	65	AO7	ADCIN-A4
		16	66		
ADCIN-B5	AO4	17	67	AO5	ADCIN-A5
		18	68		
ADCIN-B6	AO2	19	69	AO3	ADCIN-A6
		20	70		
ADCIN-B7	AO0	21	71	AO1	ADCIN-A7
		22	72		
GPIO-00, EPWM-1A	DI17	23	73	DI16	GPIO-01, EPWM-1B
GPIO-02, EPWM-2A	DI19	24	74	DI18	GPIO-03, EPWM-2B

Function	RT Box	100)-pin	RT Box	Function
GPIO-04, EPWM-3A	DI21	25	75	DI20	GPIO-05, EPWM-3B, ECAP-1
GPIO-06, EPWM-4A	DI23	26	76	DI22	GPIO-07, EPWM-4B, ECAP-2
GND		27	77		+5V in
GPIO-08, EPWM-5A, CANTX- B	DI25	28	78	DI24	GPIO-09, EPWM-5B, SCITX- B, ECAP-3
GPIO-10, EPWM-6A, CANRX- B	DI27	29	79	DI26	GPIO-11, EPWM-6B, SCIRX- B, ECAP-4
GPIO-48, ECAP5	DI29	30	80	DI28	GPIO-49, ECAP6
		31	81		
		32	82		+ 5 V
		33	83	DO0	GPIO-13, TZ-2, CANRX-B
		34	84	DO5	GPIO-14, TZ-3, SCITX-B
GPIO-24, ECAP-1, EQEPA-2	DO6	35	85	DO7	GPIO-25, ECAP-2, EQEPB-2
GPIO-26, ECAP-3, EQEPI-2	DO4	36	86		
GND		37	87		+ 5 V
		38	88		
		39	89		
GPIO-20, EQEPA-1, CANTX- B	DO2	40	90	DO3	GPIO-21, EQEPB-1, CANRX- B
		41	91	DO1	GPIO-23, EQEPI-1, SCIRX-B
GND		42	92		+ 5 V
GPIO-28, SCIRX-A		43	93		GPIO-29, SCITX-A
GPIO-30, CANRX-A		44	94		GPIO-31, CANTX-A
GPIO-32	DI31	45	95	DI30	GPIO-33
GND		46	96		+ 5 V
GND		47	97		JTAG-TDI

Function	RT Box	100	D-pin	RT Box	Function
JTAG-TCK		48	98		JTAG-TDO
JTAG-TMS		49	99		JTAG-TRSTn
JTAG-EMU1		50	100		JTAG-EMU0

Table 4.3: TI F28335 controlCARD pin map



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