THE SIMULATION PLATFORM FOR POWER ELECTRONIC SYSTEMS

PIL User Manual July 2018 - for PLECS 4.2

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PIL User Manual

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Before You Begin

Installing the PIL Demo Projects

The PLECS PIL package includes a number of demo projects to facilitate getting started with PIL. These demo projects implement typical power conversion applications such as motor drives and grid-tied inverters and are configured for different microprocessors.

Note A separate license is required to enable the PIL functionality in PLECS and access the PIL demo projects.

To install the demo projects and associated documentation in a location of your choice select **PLECS Extensions...** from the **File** menu. Then, on the **PIL** tab, configure the desired destination folder (**PIL Framework Path**) and install the packages of interest.

Note Make sure you install the **Tools** package as it contains the PIL Prep Tool – see "PIL Prep Tool" (on page 18) – which is required by most demo projects.

Included with the PIL demo projects are precompiled binaries as well as complete source code projects that can be imported into the appropriate IDE.

The source code of the PIL framework library can be obtained upon request.

What's New in this Version

Major New Features

- Support added for communication over JTAG (via GDB server).

Further Enhancements

- API modified for object-based instantiation of framework.

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Processor-in-the-Loop

As a separately licensed feature, PLECS offers support for *Processor-in-the-Loop* (PIL) simulations, allowing the execution of control code on external hardware tied into the virtual world of a PLECS model.

At the PLECS level, the PIL functionality consists of a specialized PIL block that can be found in the Processor-in-the-loop library, as well as the Target Manager, accessible from the **Window** menu. Also included with the PIL library are high-fidelity peripheral models of MCUs used for the control of power conversion systems.

On the embedded side, a *PIL Framework* library is provided to facilitate the integration of PIL functionality into your project.

Motivation

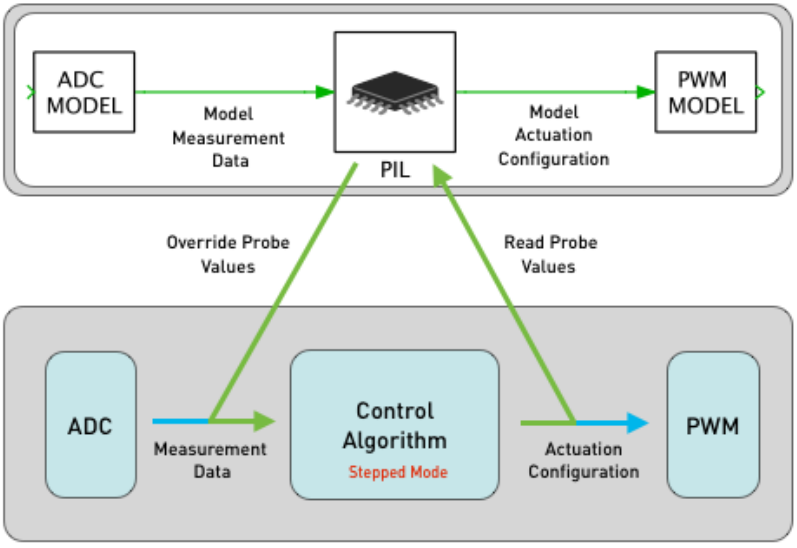
When developing embedded control algorithms, it is quite common to be testing such code, or portions thereof, by executing it inside a circuit simulator. Using PLECS, this can be easily achieved by means of a C-Script or DLL block. This approach is referred to as *Software-in-the-loop* (SIL). A SIL simulation compiles the embedded source code for the native environment of the simulation tool (e.g. Win64) and executes the algorithms within the simulation environment.

The PIL approach, on the other hand, executes the control algorithms on the real embedded hardware. Instead of reading the actual sensors of the power converter, values calculated by the simulation tool are used as inputs to the embedded algorithm. Similarly, outputs of the control algorithms executing on the processor are fed back into the simulation to drive the virtual environment. Note that SIL and PIL testing are also relevant when the embedded code is automatically generated from the simulation model.

One of the major advantages of PIL over SIL is that during PIL testing, actual compiled code is executed on the real MCU. This allows the detection of platform-specific software defects such as overflow conditions and casting errors. Furthermore, while PIL testing does not execute the control algorithms in true real-time, the control tasks *do* execute at the normal rate between two simulation steps. Therefore, PIL simulation can be used to detect and analyze potential problems related to the multi-threaded execution of control algorithms, including jitter and resource corruption. PIL testing can also provide useful metrics about processor utilization.

How PIL Works

At the most basic level, a PIL simulation can be summarized as follows:



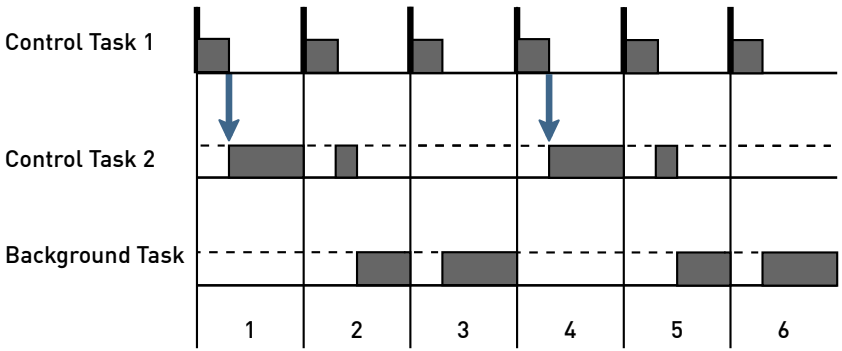
Principle of a PIL simulation

- Input variables on the target, such as current and voltage measurements, are overridden with values provided by the PLECS simulation.
- The control algorithms are executed for one control period.
- Output variables on the target, such as PWM peripheral register values, are read and fed back into the simulation.

We refer to variables on the target which are overridden by PLECS as *Override Probes*. Variables read by PLECS are called *Read Probes*.

While *Override Probes* are set and *Read Probes* are read the dispatching of the embedded control algorithms must be stopped. The controls must remain halted while PLECS is updating the simulated model. In other words, the control algorithm operates in a stepped mode during a PIL simulation. However, as mentioned above, when the control algorithms are executing, their behavior is identical to a true real-time operation. We therefore call this mode of operation *pseudo real-time*.

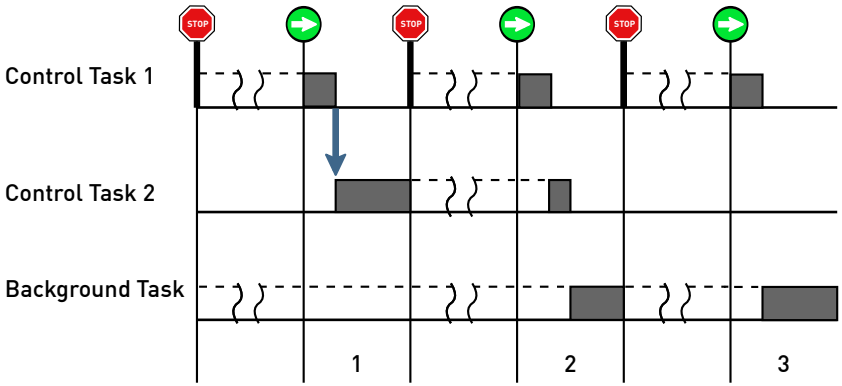
Let us further examine the pseudo real-time operation in the context of an embedded application utilizing nested control loops where fast high-priority tasks (such as current control) interrupt slower lower-priority tasks (such as voltage control). An example of such a configuration with two control tasks is illustrated in the figure below. With every hardware interrupt (bold vertical bar), the lower priority task is interrupted and the main interrupt service routine is executed. In addition, the lower priority task is periodically triggered using a software interrupt. Once both control tasks have completed, the system continues with the background task where lowest priority operations are processed. The timing in this figure corresponds to true real-time operation.



Nested Control Tasks

The next figure illustrates the timing of the same controller during a PIL simulation, with the *stop* and *go* symbols indicating when the dispatching of the control tasks is halted and resumed.

After the hardware interrupt is received, the system stops the control dispatching and enters a communication loop where the values of the Override Probes and Read Probes can be exchanged with the PLECS model. Once a new step request is received from the simulation, the task dispatching is



Pseudo real-time operation

restarted and the control tasks execute freely during the duration of one interrupt period. This pseudo real-time operation allows the user to analyze the control system in a simulation environment in a fashion that is behaviorally identical to a true real-time operation. Note that only the dispatching of the control tasks is stopped. The target itself is never halted as communication with PLECS must be maintained.

PIL Modes

The concept of using Override Probes and Read Probes allows tying actual control code executing on a real MCU into a PLECS simulation without the need to specifically recompile it for PIL.

You can think of Override Probes and Read Probes as the equivalent of test points which can be left in the embedded software as long as desired. Software modules with such test points can be tied into a PIL simulation at any time.

Often, Override Probes and Read Probes are configured to access the registers of MCU peripherals, such as analog-to-digital converters (ADCs) and pulse-width modulation (PWM) modules. Additionally, specific software modules, e.g. a filter block, can be equipped with Override Probes and Read Probes. This allows unit-testing the module in a PIL simulation isolated from the rest of the embedded code.

To permit safe and controlled transitions between real-time execution of the control code, driving an actual plant, and pseudo real-time execution, in con-

junction with a simulated plant, the following two PIL modes are distinguished:

- **Normal Operation** – Regular target operation in which PIL simulations are inhibited.
- **Ready for PIL** – Target is ready for a PIL simulation, which corresponds to a safe state with the power-stage disabled.

The transition between the two modes can either be controlled by the embedded application, for example based on a set of digital inputs, or from PLECS using the Target Manager.

Configuring PLECS for PIL

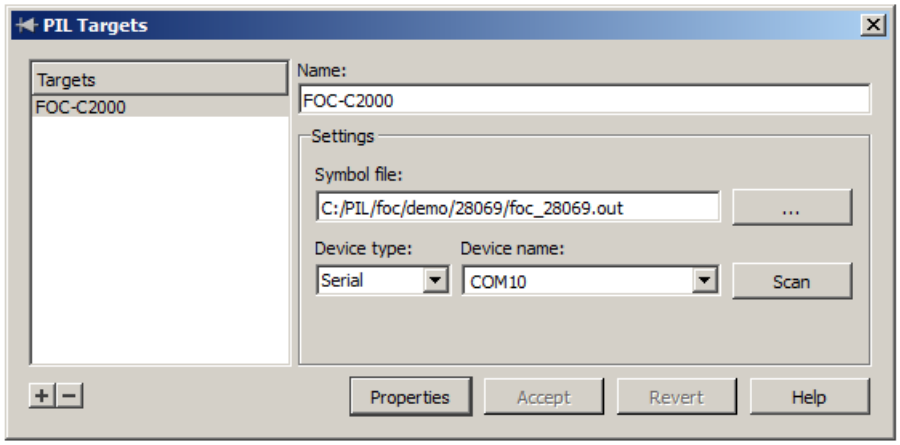
Once an embedded application is equipped with the PIL framework, and appropriate Override Probes and Read Probes are defined, it is ready for PIL simulations with PLECS.

PLECS uses the concept of *Target Configurations* to define global high-level settings that can be accessed by any PLECS model. At the circuit level, the *PIL block* is utilized to define lower level configurations such as the selection of Override Probes and Read Probes used during simulation.

This is explained in further detail in the following sections.

Target Manager

The high-level configurations are made in the *Target Manager*, which is accessible in PLECS by means of the corresponding item in the **Window** menu. The target manager allows defining and configuring targets for PIL simulation, by associating them with a symbol file and specifying the communication parameters. Target configurations are stored globally at the PLECS level and are not saved in `*.plecs` or Simulink files. An example target configuration is shown in the figure below.



Target Manager

The left hand side of the dialog window shows a list of targets that are currently configured. To add a new target configuration, click the button marked **+** below the list. To remove the currently selected target, click the button marked **-**. You can reorder the targets by clicking and dragging an entry up and down in the list.

The right hand side of the dialog window shows the parameter settings of the currently selected target. Each target configuration must have a unique **Name**.

The target configuration specifies the **Symbol file** and the communication link settings.

The symbol file is the binary file (also called “object file”) corresponding to the code executing on the target. PLECS will obtain most settings for PIL simulations, as well as the list of Override Probes and Read Probes and their attributes, from the symbol file.

Communication Links

A number of links are supported for communicating with the target. The desired link can be selected in the **Device type** combo box. For communication links that allow detecting connected devices, pressing the **Scan** button will populate the **Device name** combo box with the names of all available devices.

Serial Device

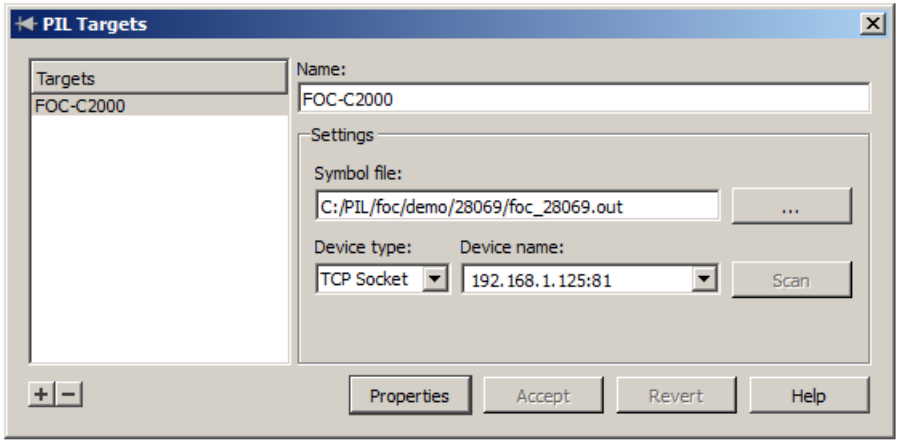
The **Serial device** selection corresponds to conventional physical or virtual serial communication ports. On a Windows machine, such ports are labeled `COMn`, where `n` is the number of the port.

FTDI Device

If the serial adapter is based on an FTDI chip, the low-level FTDI driver can be used directly by selecting the **FTD2XX** option. This device type offers improved communication speed over the virtual communication port (VCP) associated with the FTDI adapter.

TCP/IP Socket

The communication can also be routed over a TCP/IP socket by selecting the **TCP Socket** device type.



TCP/IP Communication

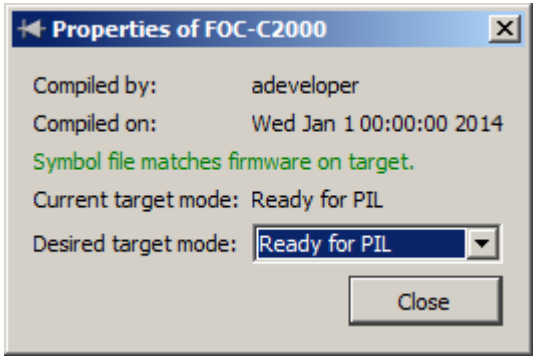
In this case the **Device name** corresponds to the IP address (or URL) and port number, separated by a colon (:).

Serial over GDB

The **Serial over GDB** device type is used in conjunction with communication over JTAG. It requires that a GDB server be running and connected to the embedded target. The configuration of this device is similar to the **TCP Socket** and consists of specifying a URL (typically the localhost 127.0.0.1) and a TCP/IP port. Please review the documentation of your GDB server for more information regarding port settings.

Target Properties

By pressing the **Properties** button, target information can be displayed as shown in the figure below.



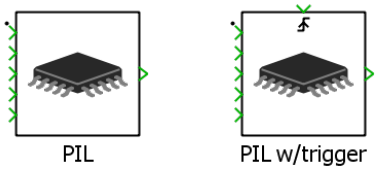
Target Properties

In addition to reading and displaying information from the symbol file, PLECS will also query the target for its identity and check the value against the one stored in the symbol file. This verifies the device settings and ensures that the correct binary file has been selected. Further, the user can request for a target mode change to configure the embedded code to run in **Normal Operation** mode or in **Ready for PIL** mode.

PIL Block

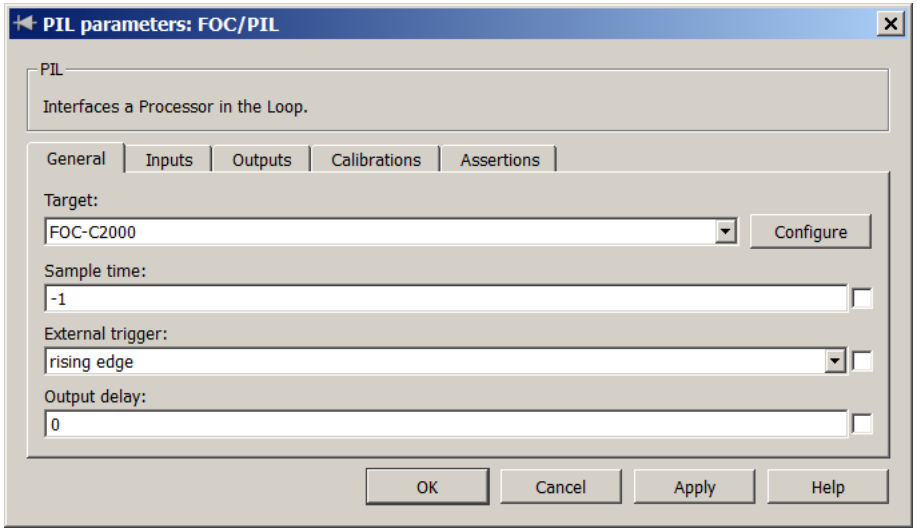
The PIL block ties a processor into a PLECS simulation by making Override Probes and Read Probes, configured on the target, available as input and out-

put ports, respectively.



PIL Block

A PIL block is associated with a target defined in the target manager, which is selected from the **Target** combo box. The **Configure...** button provides a convenient shortcut to the target manager for configuring existing and new targets.



PIL Block General Tab

The execution of the PIL block can be triggered at a fixed **Discrete-Periodic** rate by configuring the **Sample time** to a positive value. As with other PLECS components, an **Inherited** sample time can be selected by setting the parameter to **-1** or **[-1 0]**.

A trigger port can be enabled using the **External trigger** combo box. This is useful if the control interrupt source is part of the PLECS circuit, such as an

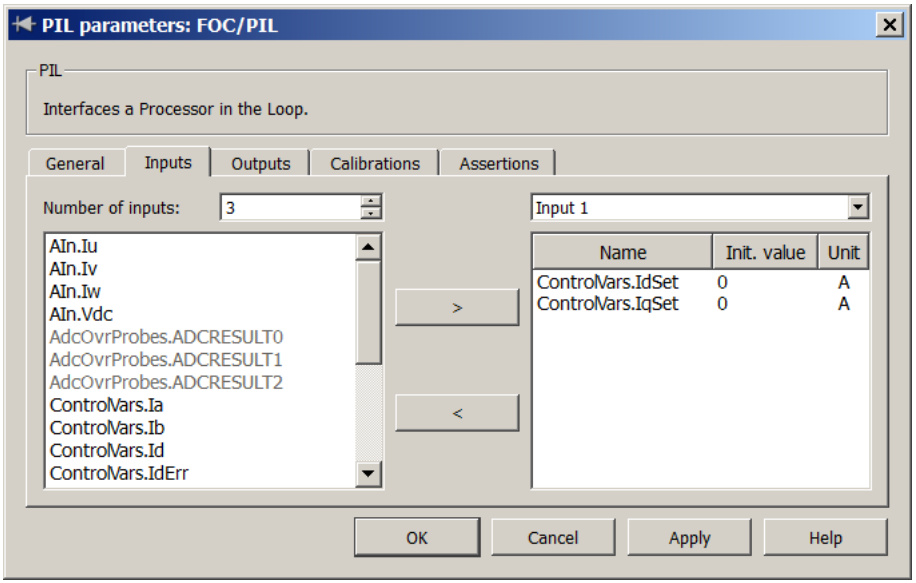
ADC or PWM peripheral model.

Typically, an **Inherited** sample time is used in combination with a trigger port. If a **Discrete-Periodic** rate is specified, the trigger port will be sampled at the specified rate.

Similar to the DLL block, the **Output delay** setting permits delaying the output of each simulation step to approximate processor calculation time.

Note Make sure the value for the **Output delay** does not exceed the sample time of the block, or the outputs will never be updated.

A delay of **0** is a valid setting, but it will create direct-feedthrough between inputs and outputs.



PIL Block Inputs Tab

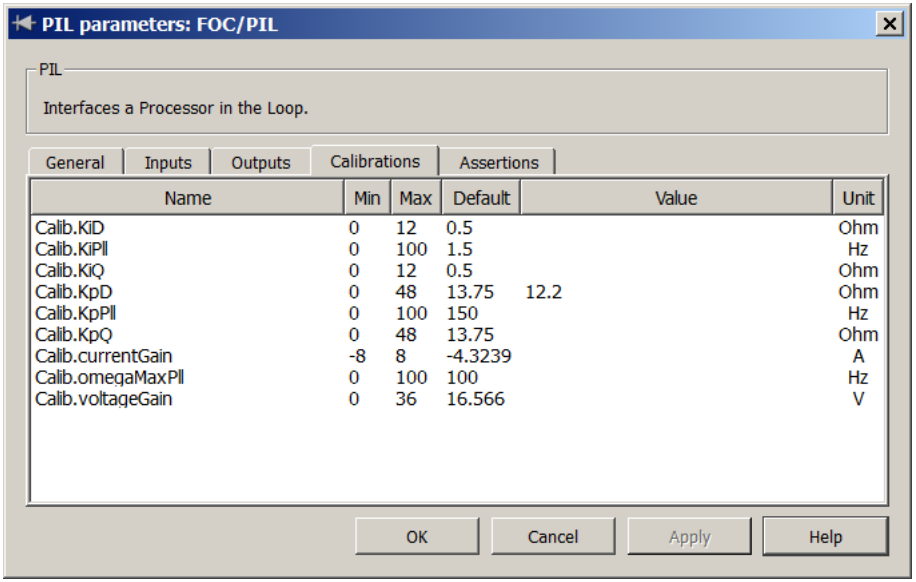
The PIL block extracts the names of Override Probes and Read Probes from the symbol file selected in the target configuration and presents lists for selection as input and output signals, as shown in the figure above.

The number of inputs and outputs of a PIL block is configurable with the **Number of inputs** and **Number of outputs** settings. To associate Override Probes or Read Probes with a given input or output, select an input/output from the combo box on the right half of the dialog. Then drag the desired Override Probes or Read Probes from the left into the area below or add them by selecting them and clicking the **>** button. To remove an Override Probe or Read Probe, select it and either press the **Delete** key or **<** button.

Note It is possible to multiplex several Override/Read Probe signals into one input/output. The sequence can be reordered by dragging the signals up and down the list.

Starting with PLECS 3.7, the PIL block allows setting initial conditions for Override Probes.

Also new with PLECS 3.7 is the Calibrations tab, which permits modifying embedded code settings such as regulator gains and filter coefficients.



PIL Block Calibrations Tab

Calibrations can be set in the **Value** column. If no entry is provided, the embedded code will use the default value as indicated in the **Default** column.

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PIL Framework

Plexim provides and maintains *PIL Frameworks* for specific processor families, which encapsulate all the necessary embedded functionality for PIL operation. Using the PIL framework, your C or C++ based embedded applications can be enabled for PIL with minimal effort.

Currently, such frameworks and associated demo applications are available for the Texas Instruments (TI) C2000™ and Microchip dsPIC33F MCU families, as well as ARM® Cortex®-M based MCUs such as STM32F and Infineon XMC devices. However, support for other platforms can be developed, as long as the following basic requirements are met:

- The code generation tools (compiler and linker) must be able to generate binary files of the ELF format containing DWARF debugging information.
- The address width of the processor cannot exceed 32 bit.
- The least addressable unit (LAU) of the processor must be no larger than 16-bit.

Overview

The fundamental operation of a PIL simulation consists of overriding and reading variables in the embedded application, and synchronizing the execution of the control task(s) with the simulation of a PLECS model. The PIL framework therefore provides the following functionality:

- Read Probes for reading the values of variables in the embedded code executing on the target and feeding the information into the simulation model.
- Override Probes for overriding variables in the embedded code with values obtained from the simulation.
- A method to uniquely identify the software executing on the target.

- A remote agent, capable of communicating with PLECS and interpreting commands related to PIL operation.
- A mechanism for stopping and starting the execution of the control tasks.
- A means to provide configuration parameters to PLECS, such as the communication baudrate.

Starting with PLECS 3.7, the PIL framework also supports *Calibrations*, which are embedded–code parameters such as filter coefficients and regulator gains. Calibrations can be modified in the PLECS environment during the initialization of a PIL simulation and allow running multiple simulations with different settings without the need for recompiling the embedded code (e.g. for the tuning of regulators).

PIL Prep Tool

To facilitate defining and configuring PIL probes and calibrations, starting with PLECS 3.7, a *PIL Prep Tool* utility is provided as part of the PIL framework.

The PIL Prep Tool parses the embedded code for PIL specific macros, and automatically generates auxiliary files to be compiled and linked with the embedded code. These auxiliary files contain functions for initializing probes and calibrations, as well as special symbols which describe to PLECS the scaling and formatting of the probes/calibrations. The generated files further include a globally unique identifier (GUID) allowing PLECS to identify the embedded code.

The PIL Prep Tool must be called as a pre-build step. Its integration into an embedded project is specific to the compiler and integrated development environment (IDE) used. Please refer to the PIL demo projects for more information.

Probes

Read Probes

Read Probes are variables in the embedded code which are configured for read access by PLECS. Any global variable can be configured as a Read Probe by means of the `PIL_READ_PROBE` macro. For example, the statement below defines and configures variable `Vdc` for read access by PLECS.

```
PIL_READ_PROBE(uint16_t , Vdc, 10, 5.0, "V");
```

The `PIL_READ_PROBE` macro results in a simple variable definition, e.g. `uint16_t Vdc`, but is also recognized by the PIL Prep Tool, which places the following statement in the auto generated file:

```
PIL_SYMBOL_DEF(Vdc, 10, 5.0, "V");
```

The `PIL_SYMBOL_DEF` macro expands into the definition of a specially formatted and statically initialized helper structure of type `const`.

```
typedef struct
{
  int q;          //!< fixed-point location
  float ref;      //!< reference value
  char *unit;     //!< unit string
} pil_var;

const pil_var PIL_V_Vdc = {10, 5.0, "V"}
```

PLECS searches for `PIL_V` symbols when parsing the binary file selected in the target manager, and uses the information of the `PIL_V` symbols to translate between the raw values stored in the Read Probe and the corresponding physical value to be used in the simulation.

In the above example, the global variable `Vdc` is configured as a Q10 with a reference of 5V. Hence, an integer value of 512 in this variable will be converted by PLECS to $\frac{512}{2^{10}} * 5\text{V} = 2.5\text{V}$.

A fixed point variable can be configured as a unitless number by using a reference value of 1.0 and setting an empty string ("") for the unit.

The same approach can be used to configure floating point variables as Read Probes.

```
PIL_READ_PROBE(float, MotorSpeed, 0, 1.0, "rpm");
```

The third parameter of the `PIL_READ_PROBE` macro, i.e. the fixed point location, is ignored with probed floating point variables. However, it is possible to specify reference values for floating point variables. For example, the macro below configures `MotorSpeed` with a reference of 1800 rpm. Hence, a value of 0.5 in this variable will be converted to $0.5 * 1800\text{rpm} = 900\text{rpm}$.

It is also possible to configure structure members, as shown below.

```
struct BATTERY {
  PIL_READ_PROBE(int16_t, voltage, 10, 5.0, "V");
};
```

Override Probes

Override Probes, i.e. variables in the embedded code that can be overridden by PLECS, are defined with the `PIL_OVERRIDE_PROBE` macro as illustrated below.

```
struct BATTERY {
  PIL_OVERRIDE_PROBE(int16_t, voltage, 10, 5.0, "V");
};

struct BATTERY MyBattery;
```

The `PIL_OVERRIDE_PROBE` macro expands into a variable definition that is augmented by two helper symbols which permit the `MyBattery.voltage` variable to be overridden by PLECS.

```
struct BATTERY {
  int16_t voltage;
  int16_t voltage_probeV;
  int16_t voltage_probeF;
};
```

While parsing a binary file for symbol information, PLECS detects variables with matching `_probeF` and `_probeV` definitions and identifies those as Override Probes.

In addition, the PIL Prep Tool will recognize the `PIL_OVERRIDE_PROBE` macro and generate the following auxiliary macro as described in the Read Probe section:

```
PIL_SYMBOL_DEF(MyBattery_voltage, 10, 5.0, "V");
```

Note Only variables defined as Override Probes are configurable as inputs for the PIL block.

An Override Probe is similar to a toggle switch with the following two states:

- **Feedthrough** – The Override Probe value is provided by the embedded application
- **Override** – The Override Probe value is provided by PLECS

The state of an Override Probe can be switched dynamically at runtime and is stored in the `_probeF` helper variable.

With this approach, the same build of the embedded application can be used to control actual hardware or be tested in a PIL simulation, by simply switching the mode of Override Probes, without recompiling.

To properly interact with PLECS, the embedded code must access the Override Probes exclusively by the following set of macros:

Override Probe Macros

Macro	Description
`INIT_OPROBE(probe)`	Initializes an Override Probe. Must be called during the initialization of the embedded program.
`SET_OPROBE(probe, value)`	Assigns a value to an Override Probe.

The PIL Prep Tool will generate a function called `PilInitOverrideProbes()` which contains `INIT_OPROBE` calls for all Override Probes. This function must be called during the initialization phase of the embedded code before any Override Probes are used.

If an Override Probe is in the feedthrough state, the **value** assigned to the macro is written into **probe**. Otherwise, the override value supplied by PLECS is used, which is stored in the `_probeV` helper variable.

An example for adding Override Probes to existing code is given in the following two listings.

```
Battery.voltage = measureBattVolt();

PLX_VECT_parkRot(ControlVars.Ia, ControlVars.Ib, \
  &ControlVars.Id, &ControlVars.Iq, \
  ControlVars.fluxPosSin, ControlVars.fluxPosCos);
```

Original code without use of Override Probes

Assume that during PIL simulations, we would like to override the variable `Battery.voltage` as well as the values of `ControlVars.Id` and `ControlVars.Iq`. While the battery voltage is updated by a simple write access, the Id and Iq variables are modified by the `PLX_VECT_parkRot(...)` function via pointers, which need special handling for the `SET_OPROBE` macro integration.

The next listing illustrates how `SET_OPROBE` is properly used in this example.

```
SET_OPROBE(Battery.voltage, measureBattVolt());

int16_t id, iq;

PLX_VECT_parkRot(ControlVars.Ia, ControlVars.Ib, \
  &id, &iq, \
  ControlVars.fluxPosSin, ControlVars.fluxPosCos);

SET_OPROBE(ControlVars.Id, id);
SET_OPROBE(ControlVars.Iq, iq);
```

Use of Override Probes

For the battery voltage, the assignment can simply be replaced by the SET_OPROBE macro. For the Id and Iq values, auxiliary variables are used, updated by the `PLX_VECT_parkRot(...)` function, and subsequently assigned to the Override Probes.

Note The `SET_OPROBE` macro must be used whenever a value is assigned to an Override Probe. A direct assignment using the equal (=) statement will result in unpredictable behavior.

Calibrations

Calibrations are variables used to configure algorithms in the embedded code, such as filter coefficients, thresholds, timeouts and regulator gains.

The PIL framework provides the `PIL_CALIBRATION` macro for a convenient definition of such calibrations. For example, the statement below declares and configures variable `Kp` as a PIL calibration.

```
PIL_CALIBRATION(int16_t, Kp, 10, 5.0, "Ohm", 0, 10.0, 0.5);
```

The first five parameters of the `PIL_CALIBRATION` macro are identical to the definition of a Read Probe. Accordingly, the macro expands into a simple variable definition `uint16_t Kp`.

The additional three parameters define the allowable range of values for the Calibration as well as its default value.

In the above example, the allowable range for Kp is $0 - 10\Omega$. Upon initialization, Kp is set to 0.5Ω.

The `PIL_CALIBRATION` macro is interpreted by the PIL Prep Tool to generate a `PIL_SYMBOL_CAL_DEF` macro. Similar to `PIL_SYMBOL_DEF`, this macro produces the necessary information for PLECS to properly interpret and handle the calibration. The PIL Prep Tool also generates a function called `PilInitCalibrations()` which sets all Calibrations to default values. This function must be called during the initialization phase of the embedded code before any calibrations are used. It is also important that this function be called in the `PIL_CLBK_TERMINATE_SIMULATION` callback to revert changes made during a PIL simulation.

Code Identity

PLECS accesses Override Probes, Read Probes and Calibrations by address (as opposed to name). The PIL block extracts the address of a given variable from the debugging information contained in the binary file supplied to the Target Manager. It is therefore important to ensure the selected binary file matches the code that is actually executing on the target, or erroneous memory locations will be accessed. This is achieved by comparing a globally unique

identifier (GUID) stored in the binary file with the value reported by the target. PLECS performs this check at the beginning of a simulation, as well as when the PIL block is opened. As explained in section "Target Manager" (on page 9), the target manager can be used to verify the match of the selected binary file.

The GUID is generated at compile time by the PIL Prep Tool. Additionally, macros for the compile time, and log-on name of the person who compiled the code are created.

```
#define CODE_GUID {0xA8,0x45,0x11,0xDE,0x05,0x4C,0xAC,0x41}
#define COMPILE_TIME_DATE_STR "Sun May 30 10:11:43 2010"
#define USER_NAME "john doe"
```

The value of `CODE_GUID` is passed to the PIL framework during initialization; see "Framework Configuration" (on page 37). The value must also be assigned to the `PIL_D_Guid` constant as follows:

```
PIL_CONST_DEF(unsigned char, Guid[], CODE_GUID);
```

The other two macros can be used for diagnostics purposes using PIL constants, as demonstrated in section "Configuration Constants" (on page 38).

Remote Agent

The *remote agent* services the communication link with PLECS and processes commands received from PLECS to access Override Probes and Read Probes, and to step the control code during a PIL simulation.

The user of the PIL framework is generally responsible for implementing the driver for a specific communication link, i.e. for configuration of hardware and basic reception and transmission of data.

Communication Callbacks

The PIL framework interacts with the application specific communication driver by *communication callback functions*.

Two callbacks exist:

- `CommCallback(...)` – Called at each system interrupt from `PIL_beginInterruptCall(...)`.
- `BackgroundCommCallback(...)` – Periodically called from `PIL_backgroundCall(...)`.

A given communication link might use either or both callbacks for its implementation. For realizing the data exchange with the framework, the user needs to utilize the serial input and output functions presented in the following section. The callback functions are registered with the framework as described on page 37.

Serial Communication

The remote agent utilizes a simple network layer with message framing and error checking, making the protocol suitable for a wide range of serial communication links such as RS-232, RS-485, TCP/IP and CAN.

To ensure no characters are dropped during a serial communication, the `CommCallback()` from the interrupt should be used to service the link.

A typical implementation of a serial communication callback is shown in the SCI callback listing.

```
void SCIPoll(PIL_Handle_t pilHandle)
{
  while(SciaRegs.SCIFFRX.bit.RXFFST != 0)
  {
    // a character has been received
    PIL_RA_serialIn(pilHandle, (int16)SciaRegs.SCIRXBUF.all);
  }

  int16_t ch;
  if(SciaRegs.SCICTL2.bit.TXRDY == 1)
  {
    // link is ready for transmission
    if(PIL_RA_serialOut(pilHandle, &ch))
    {
      SciaRegs.SCITXBUF = ch;
    }
  }
}
```

SCI callback

Notice the use of the following two functions:

- `PIL_RA_serialIn(...)` – For the reception of characters.
- `PIL_RA_serialOut(...)` – For the transmission of characters.

JTAG-based Parallel Communication

Starting with PLECS 4.2, the PIL framework also supports communication over JTAG by means of a memory-based parallel data exchange. This communication mode is substantially slower than a typical serial link, but can be useful for embedded targets that do not include peripherals/drivers for serial communication.

The implementation of this limited bandwidth communication mode is fully integrated with the PIL framework and does not require the user to provide any communication callbacks.

However, the application has to allocate a buffer in MCU memory for the data exchange and instruct PLECS of its location by means of Configuration Constants - see section “Configuration Constants” (on page 38).

```
#define PARALLEL_COM_PROTOCOL 2
#define PARALLEL_COM_BUF_ADDR 0x20004000
#define PARALLEL_COM_BUF_LEN  0x100

PIL_CONST_DEF(uint16_t, ParallelComProtocol, PARALLEL_COM_PROTOCOL);
PIL_CONST_DEF(uint32_t, ParallelComBufferAddress, PARALLEL_COM_BUF_ADDR);
PIL_CONST_DEF(uint16_t, ParallelComBufferLength, PARALLEL_COM_BUF_LEN);
PIL_CONST_DEF(uint16_t, ParallelComTimeoutMs, 200);
PIL_CONST_DEF(uint16_t, ExtendedComTimingMs, 2000);
```

Parallel Communication Configuration

Two protocols for JTAG-based parallel communication are provided by the PIL Framework:

1 JTAG access to MCU memory is made without halting the processor.

2 The processor is halted for each message exchange.

The proper choice of the protocol depends on the MCU architecture, type of emulator and associated GDB server. In case of C2000™ MCUs, the selection of protocol 1 in conjunction with C2Prog and TI emulators is recommended. For ARM® Cortex®-M based MCUs, debugged in conjunction with Segger or

OpenOCD software/hardware, protocol 2 typically achieves a higher communication throughput.

Also shown in the listing above are communication timing parameters with typical values for JTAG-based communication.

The PIL framework is configured for JTAG-based parallel configuration as follows. See also section “Framework Configuration” (on page 37).

```
PIL_configureParallelCom(PilHandle, PARALLEL_COM_PROTOCOL,
     PARALLEL_COM_BUF_ADDR, PARALLEL_COM_BUF_LEN);
```

Framework Integration and Execution

Principal Framework Calls

The PIL framework provides the following two principal functions which must be called periodically by the embedded application to enable PIL functionality:

- `PIL_beginInterruptCall(...)` – Framework call from interrupt.
- `PIL_backgroundCall(...)` – Framework call from background loop.

The `PIL_beginInterruptCall(...)` must be added at the beginning of the main interrupt service routine, while the `PIL_backgroundCall(...)` is called periodically from the background task.

The actions performed by those calls depends on whether a PIL simulation is running or not.

	Real-time	**Pseudo Real-time**
PIL_beginInterruptCall	CommCallback	CommCallback BackgroundCommClbk Message Evaluation PIL Cmd Handling
PIL_backgroundCall	BackgroundCommClbk Message Evaluation PIL Cmd Handling	N/A

Mode-specific actions during framework execution

In the following, the concept of the PIL integration is further illustrated for a TI-RTOS based application with nested control tasks (see code snippet below).

Note The PIL framework does not equire the use of a real-time operating system. A simple periodic interrupt and endless background loop are completely adequate for the execution of the framework.

```
/**
 * Main interrupt routine
 */
Void TickFxn(UArg arg)
{
  PIL_beginInterruptCall(PilHandle);

  // fast control task
  ControlTask1();

  // slow control task
  divider++;
  if(divider == TASK2_PERIOD)
  {
    divider = 0;
    Swi_post(Swi);
  }
}

/**
 * Software interrupt for slow control task
 */
Void SwiFxn(UArg arg0, UArg arg1)
{
  ControlTask2();
}

/**
 * Background task
 */
Void BackgroundTaskFxn(Void)
{
  PIL_backgroundCall(PilHandle);
}
```

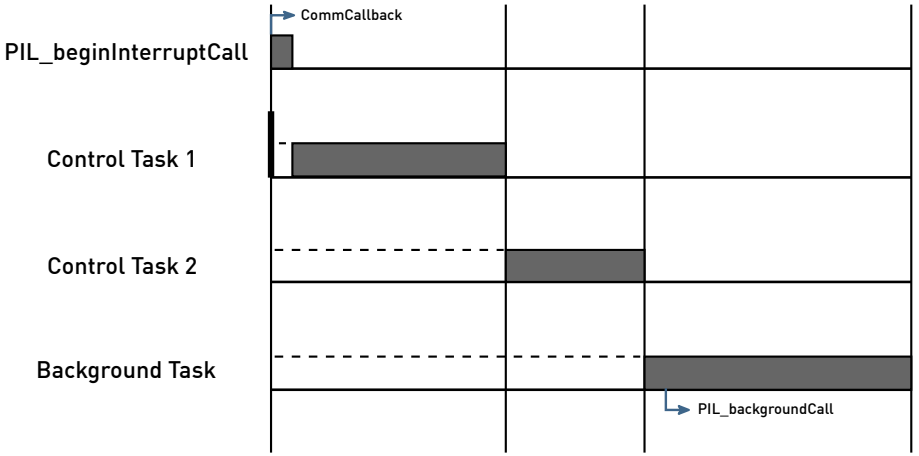
Control Task Dispatching

In this example, the first control task is triggered by a hardware interrupt related to the system counter. A divider is used to dispatch a second, lower priority task. When the divider reaches a specified value, the second control task is dispatched by a software interrupt.

Assuming the slow task takes longer than a hardware interrupt period, the second control task is interrupted several times before its execution is finished.

Now let us examine the operation of the framework in both real-time and pseudo real-time mode.

The figure on page 29 shows the framework operation in non-PIL (real-time) mode.

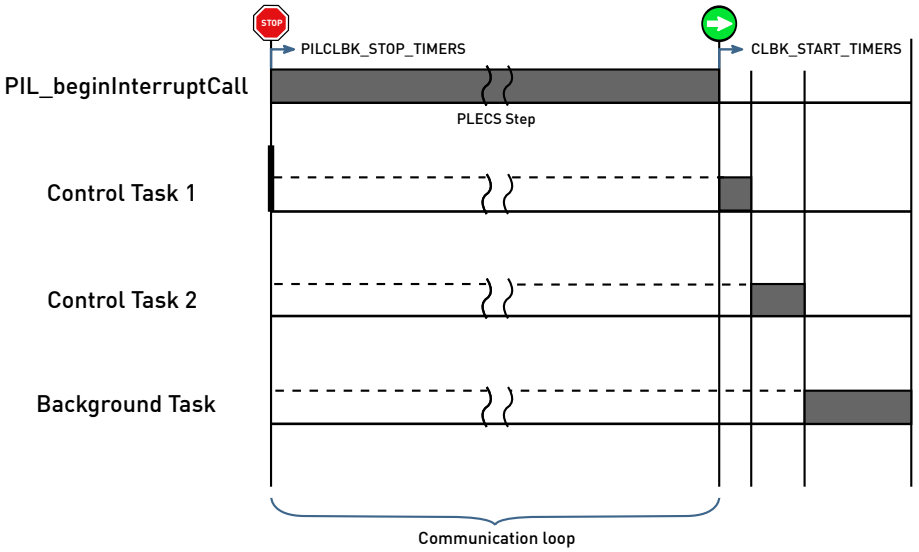


PIL framework during real-time operation

At the beginning of the hardware interrupt service routine, the `PIL_beginInterruptCall()` is executed, which, in real-time mode, only calls the registered `CommCallback` function. As already mentioned, this callback should be used to service the link for a serial communication to ensure no characters are dropped.

Note During real-time operation, the PIL framework must have a minimal influence on the timing of the dispatched control tasks. Therefore the `CommCallback` function must be implemented as efficiently as possible.

As its name suggests, `PIL_backgroundCall(...)` function is executed from the background loop, which in turn calls the `BackgroundCommCallback()`, if configured. The `PIL_backgroundCall(...)` also parses incoming messages that are buffered by the communication callback functions, and processes PIL commands.



PIL framework during pseudo real-time operation

The next figure shows the system behavior during a PIL simulation, i.e. in pseudo real-time mode, where control task execution is paced and synchronized with the simulation of a PLECS model.

At the start of the hardware interrupt service routine, the task dispatching stops and the system enters a communication loop.

In this loop, both communication callbacks and the command parsing functions are executed. This is different from true real-time mode, where the background communication callback and the command parsing functions are called from the background loop.

Once a request for a new control step is received, the framework resumes the control task dispatching and continues in free mode until the next hardware interrupt occurs. Note that in pseudo real-time operation, the `PIL_backgroundCall()` has no effect.

Control Callback

The transition between different operating modes as well as the pseudo real-time operation require application-specific actions, implemented by means of a *Control Callback*.

For example, when entering the Ready for PIL mode, the power actuation must be turned off, e.g. by disabling the PWM outputs. Also, during a PIL simulation the peripherals providing the timing to the control algorithms must be stopped and restarted, as indicated by the arrows labeled PIL_CLBK_STOP_TIMERS and PIL_CLBK_START_TIMERS.

These control actions are provided by a single callback function registered during the framework initialization, and subsequently executed with an argument specifying the specific action to be taken.

Consequently, the implementation of this callback typically consists of a `switch` statement as shown below:

```
void PilCallback(PIL_Handle_t pilHandle, PIL_CtrlCallbackReq_t aCallbackReq)
{
  switch(aCallbackReq)
  {
    case PIL_CLBK_STOP_TIMERS:
      //application specific code
      break;
    case PIL_CLBK_START_TIMERS:
      //application specific code
      break;
      .
      .
      .
    default:
      //catching an undefined callback
      break;
   }
}
```

The following control-callback actions are defined and called during the framework execution:

- `PIL_CLBK_ENTER_NORMAL_OPERATION_REQ` – Called when the target mode “Normal Operation” has been requested. The application must indicate that it has entered normal operation by executing `PIL_inhibitPilSimulation(pilHandle)`.

- `PIL_CLBK_LEAVE_NORMAL_OPERATION_REQ` – Called when the target mode "Ready for PIL" has been requested. The application must confirm that it is ready for PIL simulations by executing `PIL_allowPilSimulation(pilHandle)`.
- `PIL_CLBK_PREINIT_SIMULATION` – Called before transitioning to a PIL simulation. Can be used to reconfigure task dispatching, for example if an MCU coprocessor such as the TI CLA is to be tied into the PIL loop. Interrupts are disabled when this call is made.
- `PIL_CLBK_INITIALIZE_SIMULATION` – Called at the beginning of a PIL simulation. Used to reset the controller(s) and control task dispatching to initial conditions.
- `PIL_CLBK_TERMINATE_SIMULATION` – Called at the end of a PIL simulation.
- `PIL_CLBK_STOP_TIMERS` – Called at the beginning of the control interrupt when in PIL mode (pseudo real-time operation). Used to stop all timers and counters related to the control tasks.
- `PIL_CLBK_START_TIMERS` – Called immediately before resuming the control task(s) when in PIL mode (pseudo real-time operation). Used to restart all timers and counters related to the control tasks.

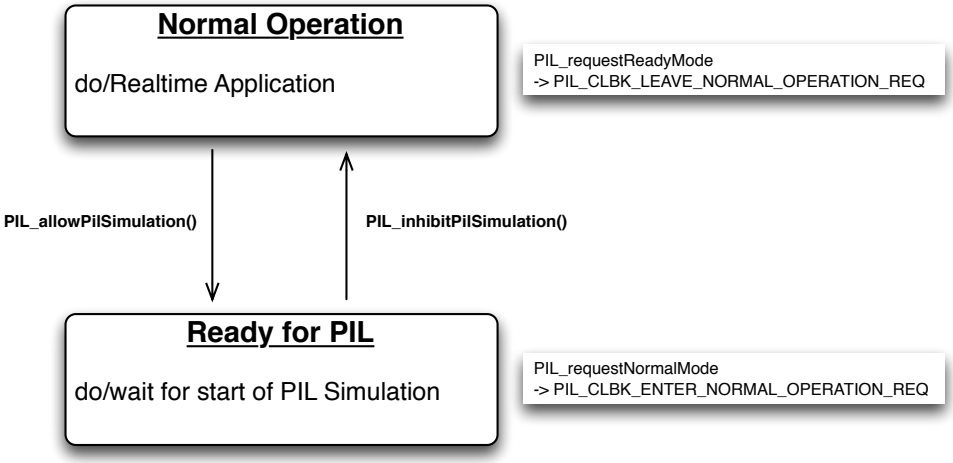
In the following sections, the different actions are further described in context of when they are called during the operation of the PIL framework. Please also review the example projects provided by Plexim for further details and control callback implementation examples.

Target Mode Switching

As described in the section "PIL Modes" (on page 8) the PIL framework distinguishes between the two target modes.

In Normal Operation mode, the target executes in true real-time operation driving the load with an active power stage. PIL simulations are inhibited in this mode due to the power stage being active. A PIL simulation can only be started if the target is in Ready for PIL mode, which corresponds to a safe state in which the power stage is disabled. As explained in the prior section, the code for enabling or disabling the power stage is application specific and must be provided by the user via the corresponding control callback.

A target mode change can be requested either from the Target Manager or from the embedded application. Depending on the requested mode, the framework executes the appropriate callback. If the requested mode is equal to the



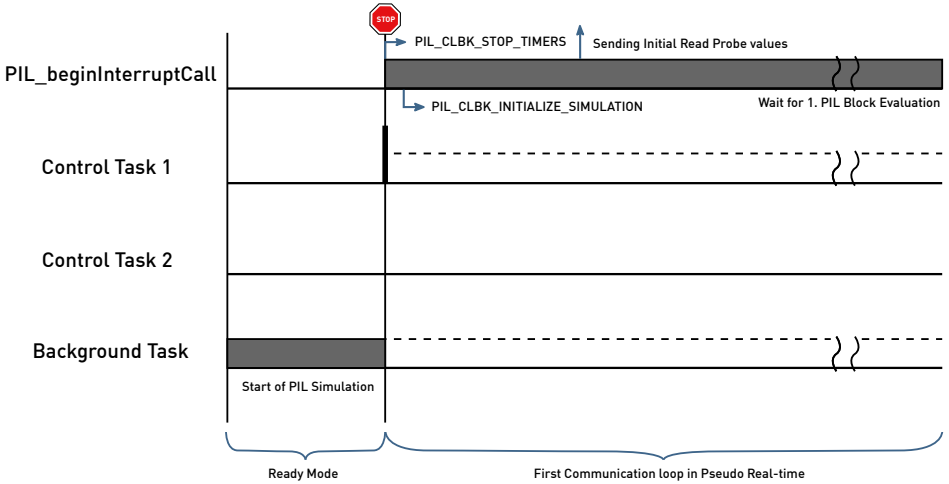
PIL target modes and mode change requests

current mode or while a PIL simulation is active, a mode request has no effect.

Target mode change requests are confirmed by the application code by calling the `PIL_allowPilSimulation()` and `PIL_inhibitPilSimualtion()` functions. Those functions also have no effect while a PIL simulation is active. Please refer to the example projects provided by Plexim for further details and implementation examples.

Simulation Start and Termination

When running multiple PIL simulations and comparing results it is important that all simulation-runs begin with identical initial conditions. This is achieved by means of the `PIL_CLBK_INITIALIZE_SIMULATION` request, which is issued via the control callback at the beginning of a simulation.



Start of a PIL Simulation

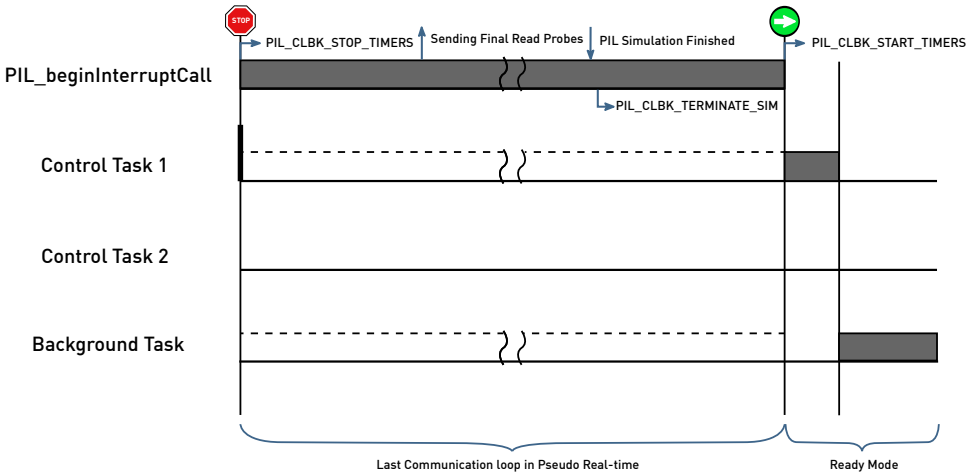
Note The initial conditions of Read Probes are fed into the PLECS model at simulation time t=0. However, these values will be immediately modified if the PIL block is also triggered at time t=0 and the output delay of the block is set to zero.

At the end of a PIL simulation, a `PIL_CLBK_TERMINATE_SIMULATION` request is issued prior to returning to real-time operation.

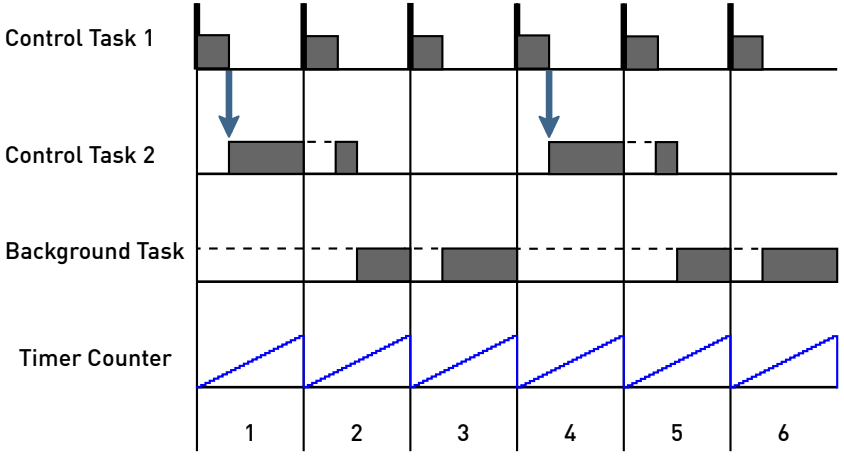
Control Dispatching

During a PIL simulation, the target operates in a pseudo real-time fashion with the execution of the control tasks being paced and synchronized with the simulation.

In the example shown in the next figure, the interrupt for Control Task 1 is based on the period of a hardware timer. Therefore, the timer period directly determines the amount of time available for the execution of the control tasks until the next interrupt occurs.



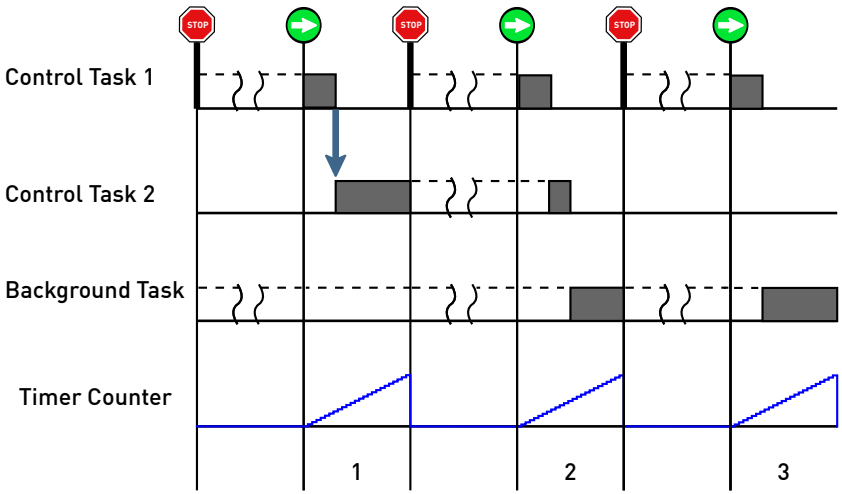
End of a PIL Simulation



Real-time operation with timer

To preserve the timing integrity in stepped mode, the hardware timer needs to be halted at the beginning of the communication loop and resumed when a step request is received, resulting in pseudo real-time operation.

By means of the CLBK_STOP_TIMERS and CLBK_START_TIMERS callback actions, the user is able to provide the necessary functionality specific to the actual application.



Pseudo real-time operation with periodically stopped timer

Task Synchronization at Start of Simulation

When control algorithms are distributed over multiple (nested) tasks, it is important to synchronize the start of a PIL simulation with the sequencing of the control tasks. In other words, after a PIL simulation has been started, a predictable and repeatable amount of time should elapse until the first execution of each nested task.

Such synchronization can be achieved by actively resetting the task dispatcher when the `PIL_CLBK_INITIALIZE_SIMULATION` request is received, as illustrated below.

```
void PilCallback(PIL_CtrlCallbackReq_t aCallbackReq)
{
  switch(aCallbackReq)
  {
    case PIL_CLBK_INITIALIZE_SIMULATION:
      //application specific code
      ...
      //active synchronization of control task dispatching
      divider = TASK2PERIOD –1;
      break;
      .
      .
      .
```

```
    default:
      //catching an undefined callback
      break;
   }
}
```

Active task synchronization via simulation initialization callback

Framework Configuration

The PIL framework data and configurations are stored in a PIL object which must be defined in the application that uses the framework.

```
/* PIL object */
PIL_Obj_t PilObj;
PIL_Handle_t PilHandle;
```

The initialization and configuration of the PIL framework consists of three mandatory steps as well as a number of optional configurations.

```
// obtain handle to PIL framework
PilHandle = PIL_init(&PilObj, sizeof(PilObj));
// set globally unique identfier
PIL_setGuid(PilHandle, PIL_GUID_PTR);
// set control callback
PIL_setCtrlCallback(PilHandle, (PIL_CtrlCallbackPtr_t)PilCallback);

// set serial communication callback
PIL_setSerialComCallback(PilHandle, (PIL_CommCallbackPtr_t)ComPoll);
```

- `PIL_init()` – Must be executed before any calls to the framework are made.
- `PIL_setGuid(...)` – Specifies the GUID to the framework .
- `PIL_setCtrlCallback(...)` – Registers the control callback for PIL simulations.

Typically, the framework is used in conjunction with a serial communication, and configured as illustrated in the code snippet above.
Additionally, the serial communication has the following optional settings:

- `PIL_setNodeAddress(...)` – Configures node address for multi-drop serial communications.
- `PIL_setBackgroundCommCallback(...)` – Registers the background communication callback.

In case of a JTAG-based parallel communication, the `PIL_configureParallelCom(...)` call is used in lieu of specifying communication callbacks.

Configuration Constants

The `PIL_CONST_DEF` macro is used for making settings and diagnostics information available to PLECS. At a minimum, `Guid[]` must be defined. If a serial link is used for communication between PLECS and the target, then it is also necessary to specify to PLECS the communication rate by means of the `BaudRate` definition. Optionally, further constants can be defined as shown below.

```
PIL_CONST_DEF(unsigned char, Guid[], CODE_GUID);
PIL_CONST_DEF(unsigned char, CompiledDate[], COMPILE_TIME_DATE_STR);
PIL_CONST_DEF(unsigned char, CompiledBy[], USER_NAME);

PIL_CONST_DEF(uint32_t, BaudRate, BAUD_RATE);
PIL_CONST_DEF(uint16_t, StationAddress, 0);
PIL_CONST_DEF(char, FirmwareDescription[], "Demo project");
```

Note Depending on the build settings it might be necessary to provide specific compiler/linker instructions (e.g. `#pragma RETAIN`) to prevent PIL definitions and constants that are not referenced by the code from being removed from the binary file.

Initialization Constants

The PIL framework also provides a mechanism to define “Initialization Constants” (or “Configurations”) that can be read from the symbol file at the beginning of a simulation and used to configure the PLECS circuit.

`PIL_CONFIG_DEF` macro is used for defining such constants. They must be of integer or float type. Strings and arrays are not supported.

```
PIL_CONFIG_DEF(uint32_t, SysClk, SYSCLK_HZ);
PIL_CONFIG_DEF(uint32_t, PwmFrequency, PWM_HZ);
PIL_CONFIG_DEF(uint32_t, ControlFrequency, CONTROL_HZ);
PIL_CONFIG_DEF(uint16_t, ProcessorPartNumber, 28069);
```

To retrieve the values of the initialization constants in PLECS use the `plecs('get', '`*path to PIL block*`', 'InitConstants')` command either in a m-file or in the model initialization commands.

```
initConstants = plecs('get','./PIL','InitConstants');

Processor = initConstants.ProcessorPartNumber;
SysClk = initConstants.SysClk;
Fs = initConstants.ControlFrequency;
Fpwm = initConstants.PwmFrequency;
```

3

TI C2000 Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

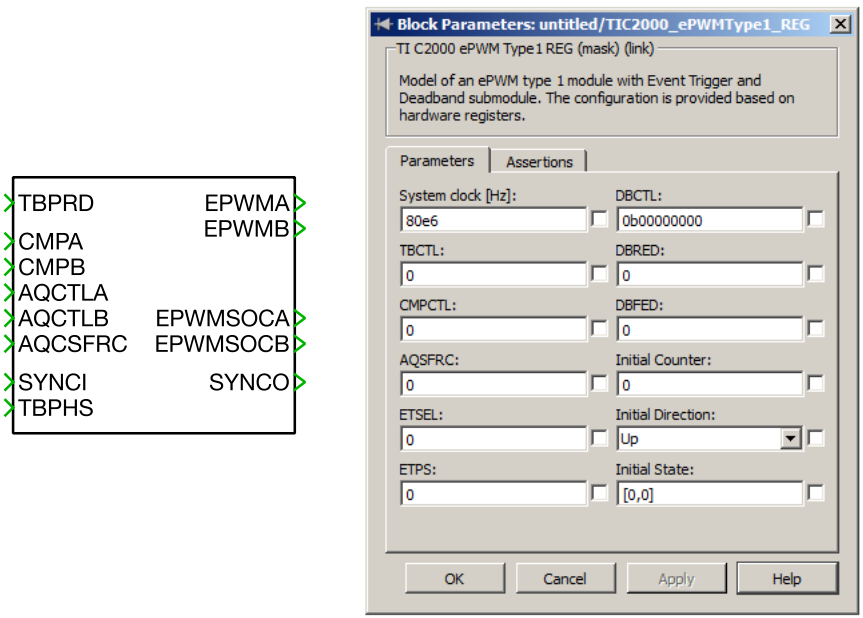
The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

Enhanced Pulse Width Modulator (ePWM) Type 1

The PLECS peripheral library provides two blocks for the TI ePWM type 0/1 module. One block has a register-based configuration mask and a second block features a graphical user interface. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during simulation and correspond to the configurations which the embedded software makes during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a graphical user interface, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.

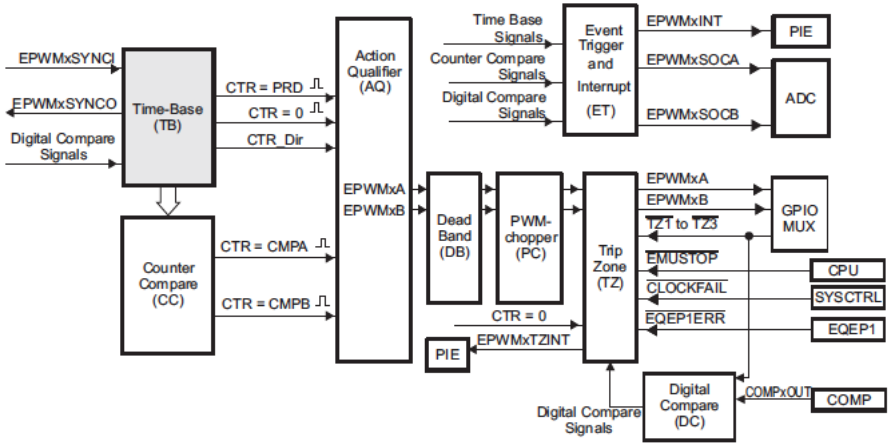


Register based ePWM module model

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Supported Submodules and Functionalities

The ePWM type 0/1 module consists of several submodules:



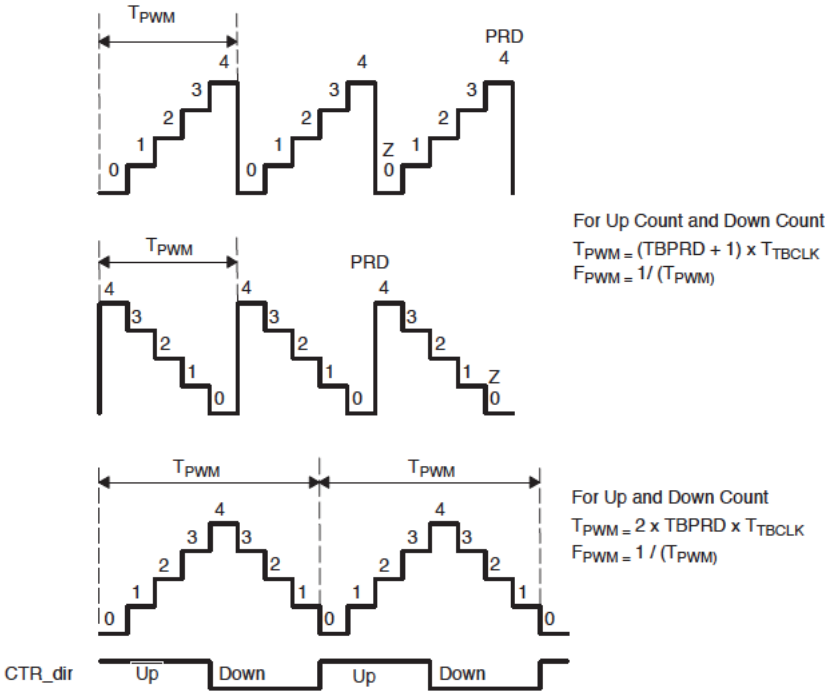
Submodules of the ePWM type 1 module [1]

The PLECS ePWM model accurately reflects the most relevant features of the following submodules:

- Time-Base submodule
- Counter-Compare submodule
- Action-Qualifier submodule
- Dead-Band submodule
- Event-Trigger submodule

Time-Base (TB) Submodule

This submodule realizes a counter that can operate in three different modes for the generation of asymmetrical and symmetrical PWM signals. The three modes, *up-count*, *down-count*, and *up-down-count*, are visualized below.



Counter modes and resulting PWM frequencies [1]

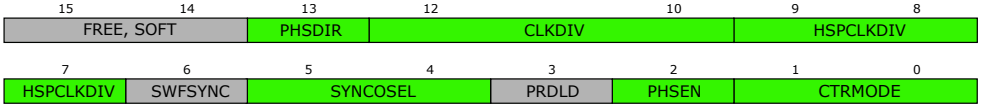
In *up-count mode*, the counter is incremented from 0 to a counter period *TBPRD* using a counter clock with period T_{TBCLK}. When the counter reaches the period, the subsequent count value is reset to zero and the sequence is repeated. When the counter is equal to zero or the period value, the submodule produces a pulse of one counter clock period, which, together with the actual counter direction, is sent to the subsequent Action Qualifier submodule.

The period of the timer clock can be calculated based on the system clock (*SYSCLKOUT*) and the two clock dividers (*CLKDIV* and *HSPCLKDIV*) by:

$$T_{TBCLK} = \frac{CLKDIV \cdot HSPCLKDIV}{SYSCLKOUT}$$

The resulting PWM period further depends on the counting mode, the counter period (*TBPRD*) and the counter clock period as depicted in the figure above.

While the system clock and the period counter value are separately defined in the mask parameters, the counter mode and the clock divider are jointly configured in the *TBCTL* register.



TBCTL Register Configuration

The *CLKDIV* and *HSPCLKDIV* cells select the desired clock dividers and the *CTRMODE* cell defines the counter mode. Only counter modes 00, 01, and 10 are supported by the PLECS ePWM model.

Initialization and Synchronization

The peripheral allows a counter and an output state initialization in the component mask. Further, the initial counter direction can be specified which only affects the up-down-count mode.

If *PHSEN* is set and a positive flank at the *SYNCI* terminal occurs, the counter is reset to *TBPHS*. When in up-down-count mode, the counter direction after a synch event is defined by the *PHSDIR* field. The initialization and synchronization features enable time-shifted pwm signals using multiple ePWM modules.

Depending on the *SYNCOSEL* settings, the *SYNCO* terminal is set for the following events:

- 00 - SYNCI
- 01 - CTR = zero
- 10 - CTR = CMPB
- 11 - Disabled

In case the *SYNCI* terminal is used for *SYNCO*, the component implements a delay as given below:

- (counter time base = system clock) - two system clock cycles
- (counter time base ! = system clock) - one counter time base cycle

Example Configuration – Step 1

This example is based on the parameter mask shown at the beginning of this chapter and will be further developed in subsequent sections. The ***TBCTL*** register is configured to:

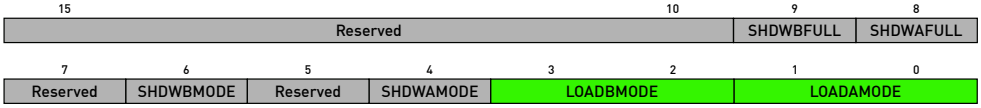
$$TBCTL = 1024 \quad \hat{=} \quad 0\,0\,0 \;\underbrace{0\,0\,1}_{CLKDIV} \;\underbrace{0\,0}_{HSPCLKDIV} \;0\,0\,0\,0\,0\,0 \;\underbrace{0\,0}_{CTRMODE}$$

According to this configuration, the time base submodule is operating in the *up-count* mode with a counter time base period twice the system clock period. The resulting PWM signal has the following period:

$$T_{PWM} = (TBPRD + 1) \cdot \frac{CLKDIV \cdot HSPCLKDIV}{SYSCLKOUT} = 187.525\ \mu s.$$

Counter-Compare (CC) Submodule

This submodule is responsible for generating the pulses *CTR* = *CMPA* and *CTR* = *CMPB* used by the Action-Qualifier submodule. In a typical application, the compare values change continuously during operation and therefore need to be part of the dynamic configuration (block inputs). The PLECS implementation only supports the shadow mode for the *CMPx* registers, i.e. the content of a *CMPx* register is only transferred to the internal configuration at reload events. The reload events are specified in the *CMPCTL* register.



CMPCTL Register Configuration

For efficiency, the PLECS ePWM model only supports the following combinations of counter mode and reload events:

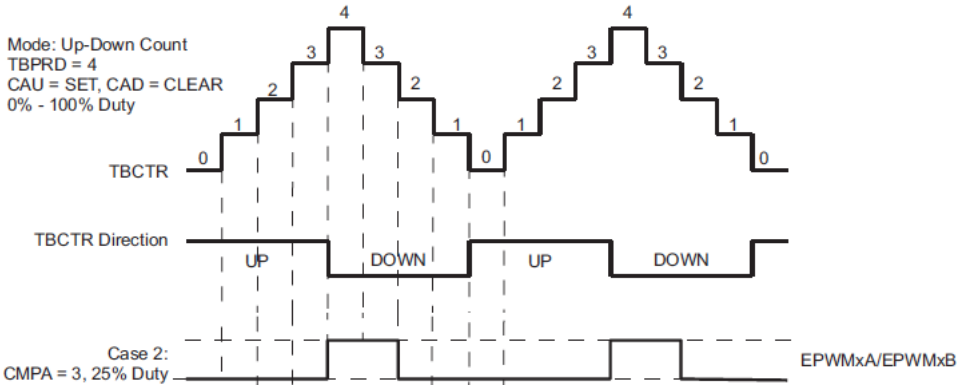
CTRMODE	LOADAMODE	LOADBMODE
Up-count	CTR = 0	CTR = 0
Down-count	CTR = PRD	CTR = PRD
Up-down-count	CTR = 0 or CTR = 0 or CTR = PRD	CTR = 0 or CTR = 0 or CTR = PRD

Furthermore, only coinciding configurations for *LOADAMODE* and *LOADBMODE* are supported.

In the example configuration, the *CMPCTL* register needs to be set to 0 because the counter is operating in up-count mode.

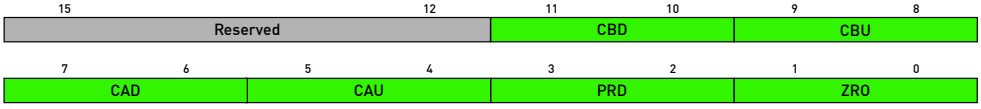
Action-Qualifier (AQ) Submodule

This submodule sets the *EPWMx* outputs based on the flags generated by the Time-Base and Counter-Compare submodules. The *AQCTLx* registers configure the actions to be performed at the different events. Similiar to the *CMPx* registers, the *AQCTLx* registers are operated in shadow mode and are reloaded at both the zero and the period event.



ePWM timing example [1]

The figure above shows an example (Case 2) where the *ePWM* output is set to high at the *CTR = CMPA* event. As depicted, an output change always lags the event by one counter clock period. The following shows the structure of the *AQCTL* register.



AQCTL Register Configuration

Actions depend on the counter direction. For example, the register cell *CBD* defines what happens to the corresponding *ePWMx* output when the counter equals *CMPB*, when the counter is counting down. The following configurations exist:

- 00 - No Action
- 01 - Force ePWMx output low
- 10 - Force ePWMx output high

- 11 - Toggle ePWMx output

If events occur simultaneously, the *ePWM* module respects a priority assignment based on the counter mode. The following figures show the Action-Qualifier prioritization.

Priority Level	Event If TBCTR is Incrementing TBCTR = Zero up to TBCTR = TBPRD	Event If TBCTR is Decrementing TBCTR = TBPRD down to TBCTR = 1
1 (Highest)	Software forced event	Software forced event
2	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
3	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
4	Counter equals zero	Counter equals period (TBPRD)
5	Counter equals CMPB on down-count (CBD)	Counter equals CMPB on up-count (CBU)
6 (Lowest)	Counter equals CMPA on down-count (CAD)	Counter equals CMPA on up-count (CBU)

Action-Qualifier prioritization in up-down-count mode [1]

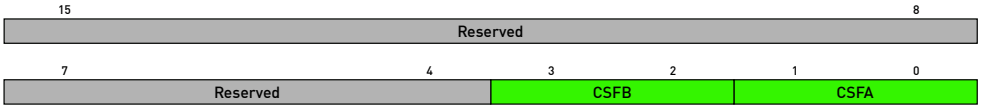
Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	Counter equal to CMPB on up-count (CBU)
4	Counter equal to CMPA on up-count (CAU)
5 (Lowest)	Counter equal to Zero

Action-Qualifier prioritization in up-count mode [1]

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

Action-Qualifier prioritization in down-count mode [1]

Notice how software-forced events have the highest priority in all three count modes. Software forcing is configured by the Action-Qualifier-Continous-Software-Force-Register (*AQCSFRC*), provided as an input to the PLECS block to allow dynamic register configuration.

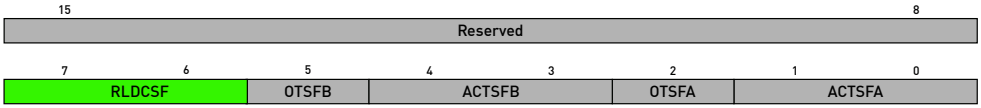


AQCSFRC Register Configuration

The figure above shows the relevant cells of the register where *CSFA* and *CSFB* can be used to force an output. The following configurations are supported:

- 00 - Forcing Disabled
- 01 - Force a continuous low on ePWMx
- 10 - Force a continuous high on ePWMx
- 11 - Forcing Disabled

As illustrated in the previous ePWM timing example, the change of an ePWMx output lags the change of *AQCSFRC* by one counter clock period. Similar to the previously described registers with dynamic configuration, the *AQCSFRC* register is operated in shadow mode. The reload events can be defined with the *AQSFRC* register.



AQSFRC Register Configuration

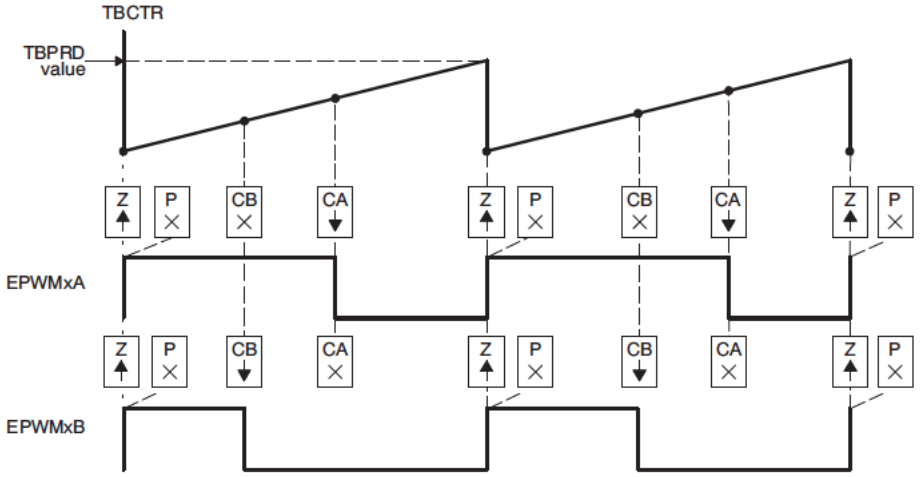
The supported modes for *RLDCSF* are listed below.

- 00 - CTR = Zero
- 01 - CTR = PRD
- 10 - CTR = Zero or CTR = PRD

Immediate mode for loading is not supported due to implementation efficiency reasons.

Example Configuration – Step 2

The following figure shows an example using the actions defined by the *AQCTL* registers. Refer to [1] for a detailed explanation of the action symbols.



Desired ePWMA and ePWMB output signals [1]

To realize the above *ePWM* signals, the dynamic configuration must be set as follows:

$$CMPA = 3500, CMPB = 2000, AQCSFRC = 0$$

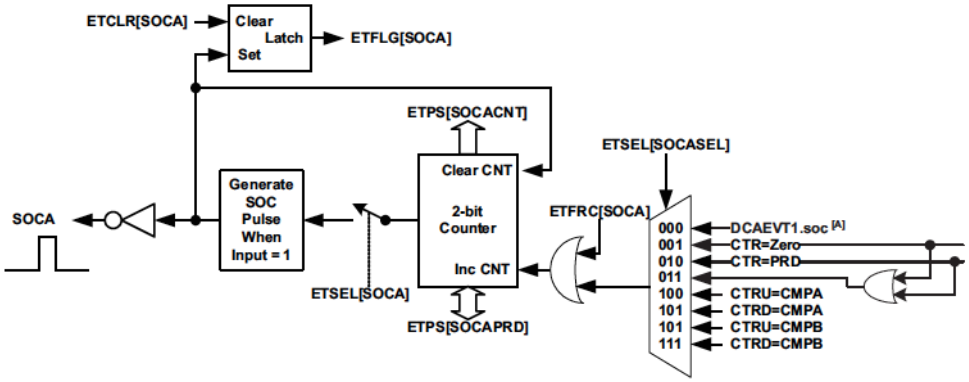
Furthermore, the Action-Qualifier must be set as shown below:

$$AQCTLA = 18 \quad \hat{=} \quad 0\,0\,0\,0 \; \underbrace{0\,0}_{CBD}\,\underbrace{0\,0}_{CBU}\;\underbrace{0\,0}_{CAD}\,\underbrace{0\,1}_{CAU}\;\underbrace{0\,0}_{PRD}\,\underbrace{1\,0}_{ZRO}$$

$$AQCTLB = 258 \quad \hat{=} \quad 0\,0\,0\,0 \; \underbrace{0\,0}_{CBD}\,\underbrace{0\,1}_{CBU}\;\underbrace{0\,0}_{CAD}\,\underbrace{0\,0}_{CAU}\;\underbrace{0\,0}_{PRD}\,\underbrace{1\,0}_{ZRO}$$

Event-Trigger (ET) Submodule

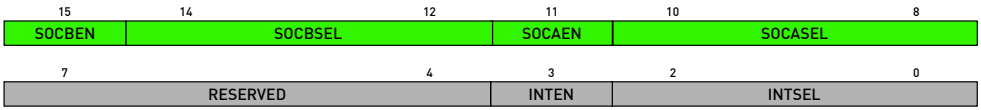
This submodule utilizes the signals generated by the Time Base and Counter Compare submodules to generate events (pulses) at the *ePWMSOCx* outputs. Such pulses can trigger an ADC conversion or invoke the execution of a control algorithm or PIL block. For each *ePWMSOC* channel, the Event Trigger module provides an internal 2-bit counter which permits a downsampling of events. The following diagram shows the internal structure for the example of *SOCA*.



Event Trigger Logic [1]

As can be seen, the counter is being incremented using one of the source signals on the right-hand side. The incrementing source signal is selected by the *SOCxSEL* field. An *SOC* pulse is generated when the *SOCxCNT* reaches its configurable period (*SOCxPRD*) and pulse generation is activated by the *SOCx* flag. The configuration for both the *SOCA* and *SOCB* portion of the Event Trigger is set by the registers *ETSEL* and *ETPS*, which are realized as static parameters of the PLECS model.

The *ETSEL* register has the following structure.

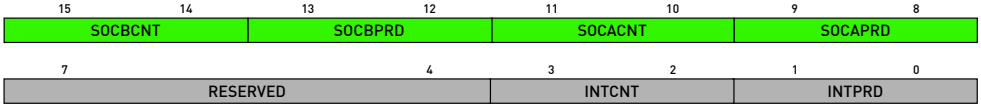


ETSEL Register Configuration

The *SOCxEN* bits activate or deactivate the *SOCx* pulses. The *SOCxSEL* cells

determine the source for the event trigger counter. Note, $SOCxSEL = 000$ is not supported in the model.

This figure shows the structure of the *ETPS* register.



ETPS Register Configuration

The *SOCxCNT* cells allow initialization of the event counter. The *SOCxPRD* bits determine the number of events that must occur before an *SOCx* pulse is generated. Refer to [1] for detailed information regarding the configuration of the *ETPS* register.

Example Configuration – Step 3

A possible use case for the Event-Trigger submodule is to generate a *SOCA* pulse every second time the TB-counter meets the *CMPA* value. To achieve this behavior, the ET is configured as follows.

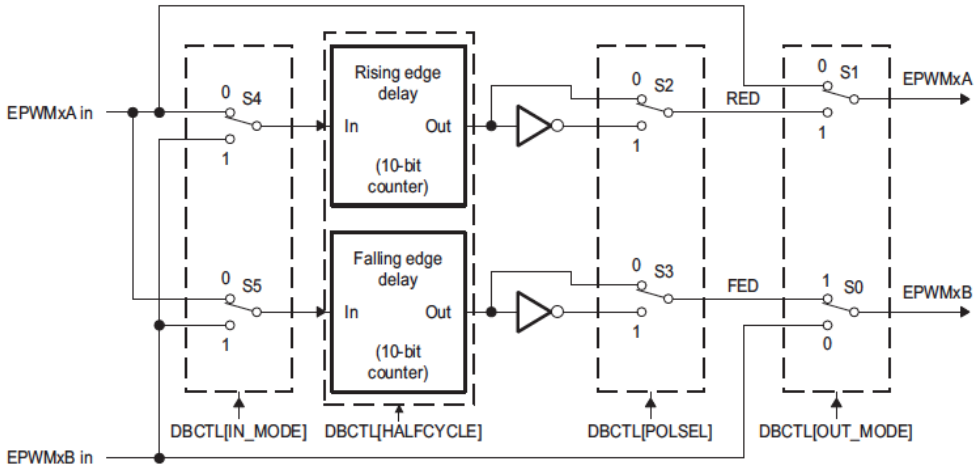
$$ETSEL = 0xC00 \;\hat{=}\; 0000 \;\underbrace{1}_{SOCAEN}\; \underbrace{100}_{SOCASEL} \;0000\;0000$$

This setting enables the *SOCA* pulses and uses the *CTR = CMPA* event for incrementing the ET-counter. Note that *SOCB* pulses are completely disabled in this example.

$$ETPS = 512 \;\hat{=}\; 0000 \;\underbrace{00}_{SOCACNT}\; \underbrace{10}_{SOCAPRD} \;0000\;0000$$

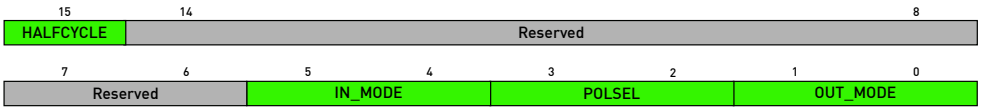
Dead-Band Submodule

The role of this submodule is to add programmable delays to rising and falling edges of the *ePWM* signals and to generate signal pairs with configurable polarity. The figure below depicts the internal structure of the Dead-Band submodule.



Dead-Band Logic [1]

As shown, the *PWMx* signals from the Action-Qualifier submodule are post-processed based on the *DBCTL* register settings. Furthermore, the delay times are programmables by the registers *DBRED* and *DBFED* for the rising and falling edge delay, respectively. The structure of the *DBCTL* register is shown in the following block diagram.



DBCTL Register Configuration

The submodule register cells allow for the following settings:

- *HALFCYCLE* - Delay counters increment with half TB-counter clock period
- *IN_MODE* - Choose source for delay counters; can also be used for output switching

- *POL_SEL* - Invert output polarity
- *OUT_MODE* - Enables Dead-Band bypassing for both outputs

Refer to [1] for detailed information regarding the configuration of the *DBCTL* register.

Example Configuration – Step 4

In the sample configuration, the signal *EPWMB* is selected as the source for both delay counters. Further, both the rising and falling edge of the outputs are delayed by 10 counter clock periods and the polarities are not inverted. The *DBCTL* register therefore should be configured as follows.

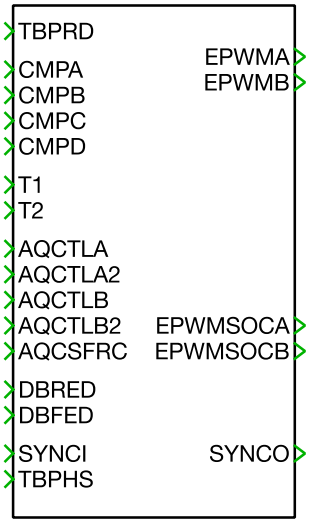
$$DBCTL = 0b110011 \;\hat{=}\; 0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \quad \underbrace{1\,1}_{IN\_MODE} \quad \underbrace{0\,0}_{POL\_SEL} \quad \underbrace{1\,1}_{OUT\_MODE}$$

With the *HALFCYCLE* bit set to zero, the *DBRED* and *DBFED* must be configured to:

$$DBRED = 10 \;\;,\;\; DBFED = 10$$

Enhanced Pulse Width Modulator (ePWM) Type 4

The PLECS peripheral library provides two blocks for the TI ePWM type 4 module. One block has a register-based configuration mask and a second block features a graphical user interface. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during simulation and correspond to the configurations which are initialized by the embedded software at startup. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a graphical user interface, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.

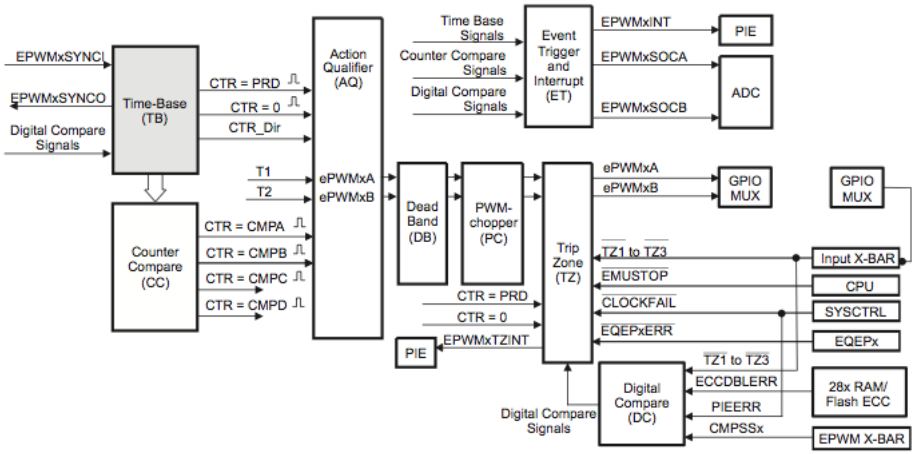


Register based ePWM module model

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Supported Submodules and Functionalities

The ePWM type 4 module consists of several submodules:



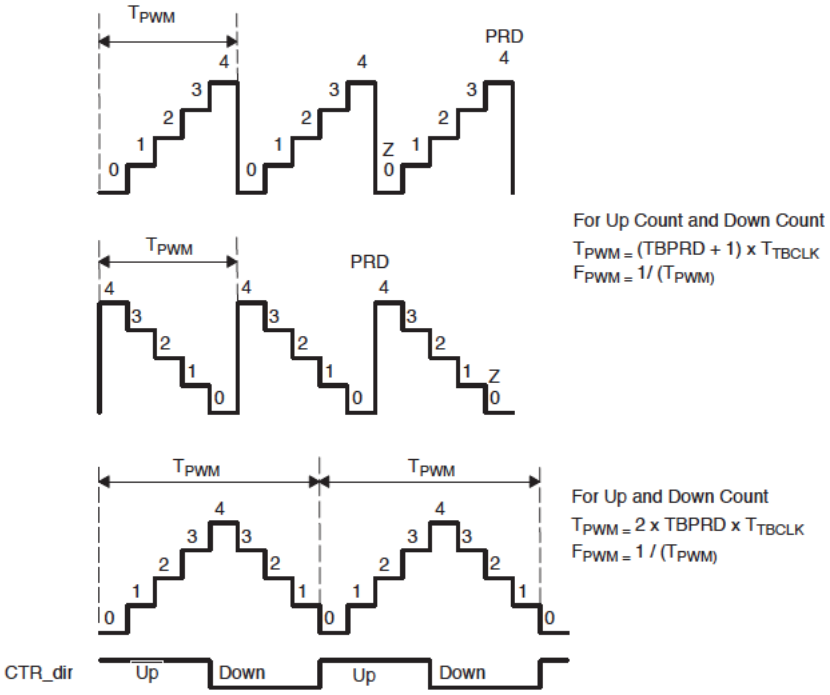
Submodules of the ePWM type 4 module [4]

The PLECS ePWM model accurately reflects the most relevant features of the following submodules:

- Time-Base submodule
- Counter-Compare submodule
- Action-Qualifier submodule
- Dead-Band submodule
- Event-Trigger submodule

Time-Base (TB) Submodule

This submodule realizes a counter that can operate in three different modes for the generation of asymmetrical and symmetrical PWM signals. The three modes, *up-count*, *down-count*, and *up-down-count*, are visualized below.



Counter modes and resulting PWM frequencies [4]

In *up-count mode*, the counter is incremented from 0 to a counter period *TBPRD* using a counter clock with period T_{TBCLK}. When the counter reaches the period, the subsequent count value is reset to zero and the sequence is repeated. When the counter is equal to zero or the period value, the submodule produces a pulse of one counter clock period, which, together with the actual counter direction, is sent to the subsequent Action Qualifier submodule.

In the type 4 ePWM module, the system clock (*SYSCLKOUT*) can be divided further to generate the EPWM clock (*EPWMCLK*). This is determined by the *EPWMCLKDIV* bit in the *PERCLKDIVSEL* register and the system clock by the following formula:

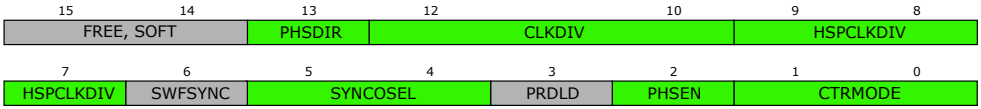
$$EPWMCLK = \frac{SYSCLKOUT}{1 + EPWMCLKDIV}$$

The period of the timer-base module clock (*TBCLK*) can be calculated based on the EPWM clock (*EPWMCLK*) and the two clock dividers (*CLKDIV* and *HSPCLKDIV*) by:

$$T_{TBCLK} = \frac{CLKDIV \cdot HSPCLKDIV}{EPWMCLK}$$

The resulting PWM period further depends on the counting mode, the counter period (*TBPRD*) and the counter clock period as depicted in the figure above.

While the system clock and the period counter value are separately defined in the mask parameters, the counter mode and the clock divider are jointly configured in the *TBCTL* register.



TBCTL Register Configuration

The *CLKDIV* and *HSPCLKDIV* cells select the desired clock dividers and the *CTRMODE* cell defines the counter mode.

Only counter modes 00, 01, and 10 are supported by the PLECS ePWM type 4 model.

Initialization and Synchronization

The peripheral allows a counter and an output state initialization in the component mask. Further, the initial counter direction can be specified which only affects the up-down-count mode.

If *PHSEN* is set and a positive flank at the *SYNCI* terminal occurs, the counter is reset to *TBPHS*. When in up-down-count mode, the counter direction after a synch event is defined by the *PHSDIR* field. The initialization and synchronization features enable time-shifted pwm signals using multiple ePWM modules.

Depending on the *SYNCOSEL* settings, the *SYNCO* terminal is set for the following events:

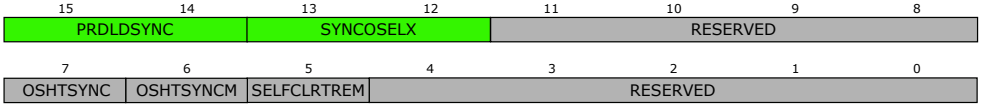
- 00 - SYNCI
- 01 - CTR = zero

- 10 - CTR = CMPB
- 11 - SYNCO is defined by *TBCTL2.SYNCOSELX*

In case the *SYNCI* terminal is used for *SYNCO*, the component implements a delay as given below:

- (counter time base = system clock) - two system clock cycles
- (counter time base ! = system clock) - one counter time base cycle

The *TBCTL2* register extends the SYNCO options and provides additional settings for reloading the period register.



TBCTL2 Register Configuration

The *SYNCOSELX* configuration only has an effect if *TBCTL.SYNCOSEL* is set to 11 and defines the *SYNCO* event:

- 00 - Disabled
- 01 - CTR = CMPC
- 10 - CTR = CMPD
- 11 - Reserved

The *PRDLDSYNC* field defines the event for reloading the active period register.

- 00 - Only at the CTR = 0 event
- 01 - At both the SYNC and the CTR = 0 event
- 10 - Only at the SYNC event
- 11 - Reserved

Example Configuration – Step 1

This example is based on the parameter mask shown at the beginning of this chapter and will be further developed in subsequent sections.

The counter time base period is set equal to the system clock period by configuring the *EPWMCLKDIV* bit to zero.

The *TBCTL* register is configured to:

$$TBCTL = 1024 \quad \hat{=} \quad 0\,0\,0 \;\underbrace{0\,0\,1}_{CLKDIV} \;\underbrace{0\,0}_{HSPCLKDIV} \;0\,0\,0\,0\,0\,0 \;\underbrace{0\,0}_{CTRMODE}$$

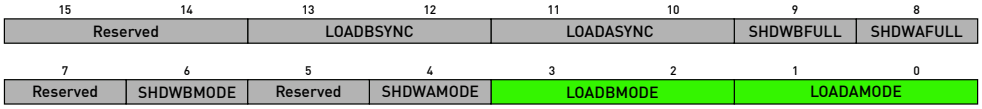
According to this configuration, the time-base submodule is operating in the *up-count* mode with a timer clock period twice the EPWM-clock period. The resulting PWM signal has the following period:

$$T_{PWM} = (TBPRD + 1) \cdot \frac{CLKDIV \cdot HSPCLKDIV}{EPWMCLK} = 187.525\ \mu s.$$

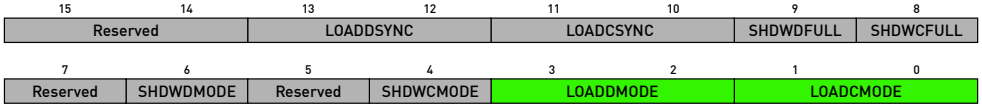
Counter-Compare (CC) Submodule

This submodule is responsible for generating the pulses *CTR* = *CMPA*, *CTR* = *CMPB*, *CTR* = *CMPC* and *CTR* = *CMPD* used by the Action-Qualifier submodule. In a typical application, the compare values change continuously during operation and therefore need to be part of the dynamic configuration (block inputs). The PLECS implementation only supports the shadow mode for the *CMPx* registers, i.e. the content of a *CMPx* register is only transferred to the internal configuration at reload events.

The reload events are specified in the *CMPCTL* and *CMPCTL2* registers.



CMPCTL Register Configuration



CMPCTL Register Configuration

For efficiency, the PLECS ePWM model only supports the following combinations of counter mode and reload events:

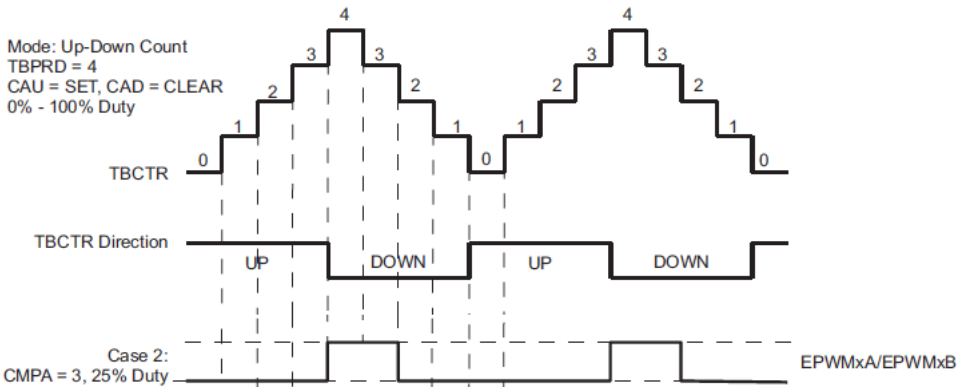
CTRMODE	LOADAMODE	LOADBMODE	LOADCMODE	LOADDMODE
Up-count	CTR = 0	CTR = 0	CTR = 0	CTR = 0
Down-count	CTR = PRD	CTR = PRD	CTR = PRD	CTR = PRD
Up-down-count	CTR = 0 or CTR = 0 or CTR = PRD	CTR = 0 or CTR = 0 or CTR = PRD	CTR = 0 or CTR = 0 or CTR = PRD	CTR = 0 or CTR = 0 or CTR = PRD

Furthermore, only coinciding configurations for *LOADAMODE*, *LOADBMODE*, *LOADCMODE* and *LOADDMODE* are supported.

In the example configuration, the *CMPCTL* and *CMPCTL2* registers need to be set to 0 because the counter is operating in up-count mode.

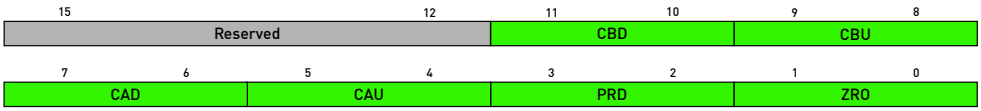
Action-Qualifier (AQ) Submodule

This submodule sets the *EPWMx* outputs based on the flags generated by the Time-Base and Counter-Compare submodules. The *AQCTLx* and *AQCTLx2* registers configure the actions to be performed at the different events. Similiar to the *CMPx* registers, the *AQCTLx* and *AQCTLx2* registers are operated in shadow mode and are reloaded at both the zero and the period events.



ePWM timing example [4]

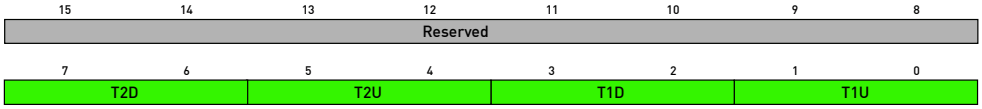
The figure above shows an example (Case 2) where the *ePWM* output is set to high at the *CTR = CMPA* event. As depicted, an output change always lags the event by one counter clock period. The following shows the structure of the *AQCTLx* register.



AQCTLx Register Configuration

An output change can also be made using the T1 and T2 events. The *AQCTLx2* register can be configured to change output when a T1 or T2 event occurs and depending on the direction of the counter at that instant. It is assumed that an output change always lags the event by one counter clock period. The following figure shows the structure of the *AQCTLx2* register.

Actions depend on the counter direction. For example, the register cell *CBD* defines what happens to the corresponding *ePWMx* output when the counter



AQCTLx2 Register Configuration

equals *CMPB*, and when the counter is counting down. The following configurations exist:

- 00 - No Action
- 01 - Force ePWMx output low
- 10 - Force ePWMx output high
- 11 - Toggle ePWMx output

If events occur simultaneously, the *ePWM* module respects a priority assignment based on the counter mode. The following figures show the Action-Qualifier prioritization.

Priority Level	Event If TBCTR is Incrementing TBCTR = Zero up to TBCTR = TBPRD	Event If TBCTR is Decrementing TBCTR = TBPRD down to TBCTR = 1
1 (Highest)	Software forced event	Software forced event
2	T1 on up-count (T1U)	T1 on down-count (T1D)
3	T2 on up-count (T2U)	T2 on down-count (T2D)
4	Counter equals CMPB on up-count (CBU)	Counter equals CMPB on down-count (CBD)
5	Counter equals CMPA on up-count (CAU)	Counter equals CMPA on down-count (CAD)
6	Counter equals zero	Counter equals period (TBPRD)
7	T1 on down-count (T1D)	T1 on up-count (T1U)
8	T2 on down-count (T2D)	T2 on up-count (T2U)
9	Counter equals CMPB on down-count (CBD)	Counter equals CMPB on up-count (CBU)
10 (Lowest)	Counter equals CMPA on down-count (CAD)	Counter equals CMPA on up-count (CBU)

Action-Qualifier prioritization in up-down-count mode [4]

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to period (TBPRD)
3	T1 on up-count (T1U)
4	T2 on up-count (T2U)
5	Counter equal to CMPB on up-count (CBU)
6	Counter equal to CMPA on up-count (CAU)
7 (Lowest)	Counter equal to Zero

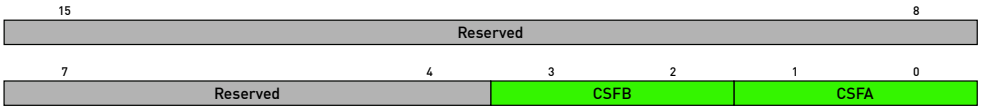
Action-Qualifier prioritization in up-count mode [4]

Notice how software-forced events have the highest priority in all three count modes. Software forcing is configured by the Action-Qualifier-Continous-Software-Force-Register (*AQCSFRC*), provided as an input to the PLECS block to allow dynamic register configuration.

Priority Level	Event
1 (Highest)	Software forced event
2	Counter equal to Zero
3	T1 on down-count (T1D)
4	T2 on down-count (T2D)
3	Counter equal to CMPB on down-count (CBD)
4	Counter equal to CMPA on down-count (CAD)
5 (Lowest)	Counter equal to period (TBPRD)

Action-Qualifier prioritization in down-count mode [4]

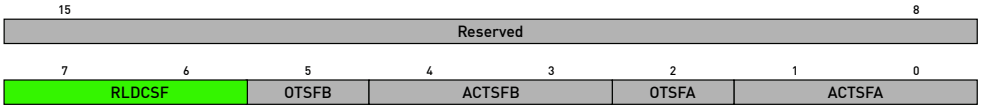
The figure below shows the relevant cells of the register where *CSFA* and *CSFB* can be used to force an output. The following configurations are supported:



AQCSFRC Register Configuration

- 00 - Forcing Disabled
- 01 - Force a continuous low on ePWMx
- 10 - Force a continuous high on ePWMx
- 11 - Forcing Disabled

As illustrated in the previous ePWM timing example, the change of an ePWMx output lags the change of *AQCSFRC* by one counter clock period. Similar to the previously described registers with dynamic configuration, the *AQCSFRC* register is operated in shadow mode. The reload events can be defined with the *AQSFRC* register.



AQSFRC Register Configuration

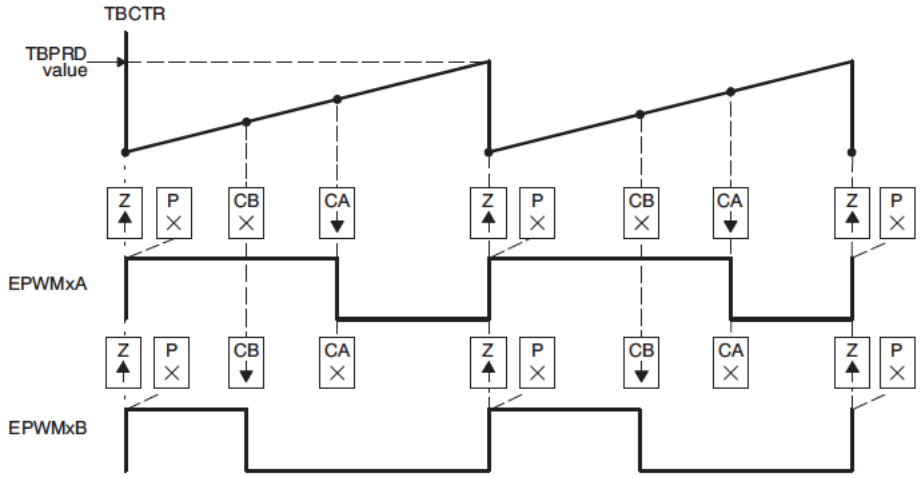
The supported modes for *RLDCSF* are listed below.

- 00 - CTR = Zero
- 01 - CTR = PRD
- 10 - CTR = Zero or CTR = PRD

Immediate mode for loading is not supported due to implementation efficiency reasons.

Example Configuration – Step 2

The following figure shows an example using the actions defined by the *AQCTLx* registers. Refer to [4] for a detailed explanation of the action symbols.



Desired ePWMA and ePWMB output signals [4]

To realize the above *ePWM* signals, the dynamic configuration must be set as follows:

$$CMPA = 3500; CMPB = 2000; AQCSFRC, AQCTLA2, AQCTLB2 = 0$$

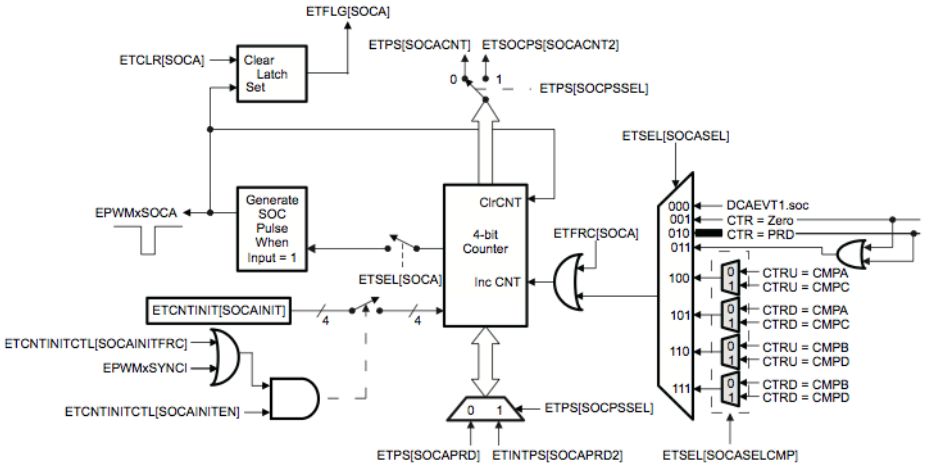
Furthermore, the Action-Qualifier must be set as shown below:

$$AQCTLA = 18 \quad \hat{=} \quad 0\,0\,0\,0 \; \underbrace{0\,0}_{CBD} \; \underbrace{0\,0}_{CBU} \; \underbrace{0\,0}_{CAD} \; \underbrace{0\,1}_{CAU} \; \underbrace{0\,0}_{PRD} \; \underbrace{1\,0}_{ZRO}$$

$$AQCTLB = 258 \quad \hat{=} \quad 0\,0\,0\,0 \; \underbrace{0\,0}_{CBD} \; \underbrace{0\,1}_{CBU} \; \underbrace{0\,0}_{CAD} \; \underbrace{0\,0}_{CAU} \; \underbrace{0\,0}_{PRD} \; \underbrace{1\,0}_{ZRO}$$

Event-Trigger (ET) Submodule

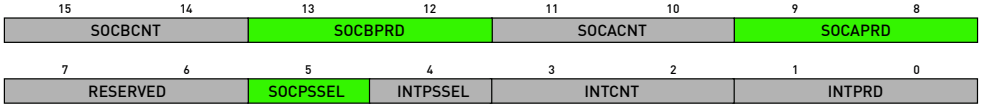
This submodule utilizes the signals generated by the Time Base and Counter Compare submodules to generate events (pulses) at the *ePWMSOCx* outputs. Such pulses can trigger an ADC conversion or invoke the execution of a control algorithm or PIL block. For each *ePWMSOC* channel, the Event Trigger module provides an internal 4-bit counter which permits a downsampling of events. The following diagram shows the internal structure for the example of *SOCA*.



Event Trigger Logic [4]

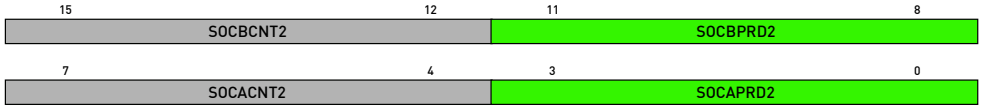
As can be seen, the counter is being incremented using one of the source signals on the right-hand side.

The figures below show the structure of the *ETPS* and *ETSOCPS* registers.



ETPS Register Configuration

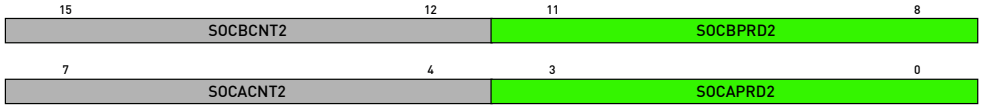
The *SOCPSSEL* bit determines whether *SOCxCNT* and *SOCxPRD* take control or whether *SOCxCNT2* and *SOCxPRD2*, in the *ETSOCPS* register, take control.



ETSOCPS Register Configuration

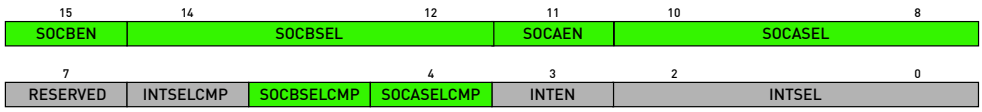
The *SOCxPRD* and *SOCxPRD2* bits determine the number of events that must occur before an *SOCx* pulse is generated. Refer to [4] for detailed information regarding the configuration of the *ETPS* and *ETSOCPS* registers.

The *ETCNTINIT* register is used to initialize the counter for the *SOCA* and *SOCB* events at startup. The structure of the register is shown below.



ETSOCPS Register Configuration

The *ETSEL* register has the following structure.



ETSEL Register Configuration

The *SOCxEN* bits activate or deactivate the *SOCx* pulses. The *SOCxSEL* cells determine the source for the event trigger counter. The *SOCxSELCMP* cells determine if *CMPA* and *CMPB* or *CMPC* and *CMPD* are used for *SOCxSEL* counter.

Note, $SOCxSEL = 000$ is not supported in the model.

The incrementing source signal is selected by the *SOCxSEL* field and the *SOCPSSEL* bit determines which counter to use. An *SOC* pulse is generated when the SOC counter (*SOCxCNT* or *SOCxCNT2*) reaches its configurable period (*SOCxPRD* or *SOCxPRD2*) and pulse generation is activated by the *SOCx* flag. The configuration for both the *SOCA* and *SOCB* portion of the Event Trigger is set by the registers *ETSEL*, *ETPS*, *ETSOCPS*, and *ETCNTINIT* registers, which are realized as static parameters of the PLECS model.

Example Configuration – Step 3

A possible use case for the Event-Trigger submodule is to generate a *SOCA* pulse every second time the TB-counter meets the *CMPA* value. To achieve this behavior, the ET is configured as follows.

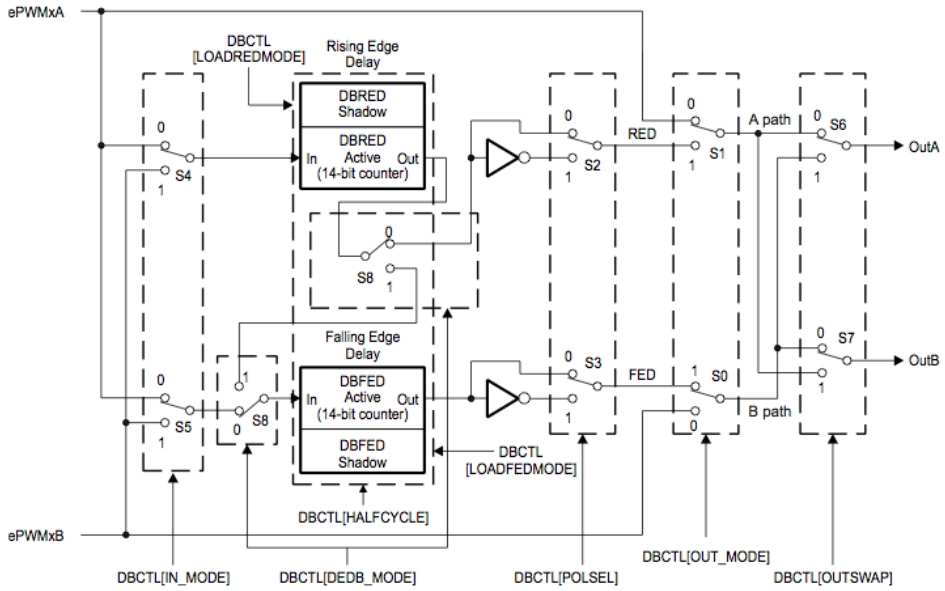
$$ETSEL = 0xC00 \quad \hat{=} \quad 0\,0\,0\,0 \quad \underbrace{1}_{SOCAEN} \quad \underbrace{1\,0\,0}_{SOCASEL} \quad 0\,0\,0 \quad \underbrace{0}_{SOCASELCMP} \quad 0\,0\,0\,0$$

This setting enables the *SOCA* pulses and uses the *CTR = CMPA* event for incrementing the ET-counter. Note that *SOCB* pulses are completely disabled in this example.

$$ETPS = 512 \quad \hat{=} \quad 0\,0\,0\,0\;0\,0 \quad \underbrace{1\,0}_{SOCAPRD} \quad 0\,0 \quad \underbrace{0}_{SOCPSSEL} \quad 0 \quad 0\,0\,0\,0$$

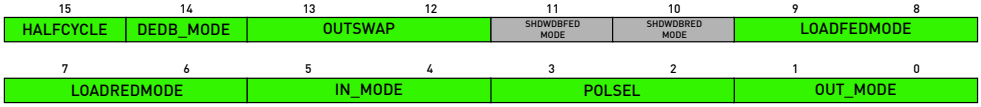
Dead-Band Submodule

The role of this submodule is to add programmable delays to rising and falling edges of the *ePWM* signals and to generate signal pairs with configurable polarity. The figure below depicts the internal structure of the Dead-Band submodule.



Dead-Band Logic [4]

As shown, the *PWMx* signals from the Action-Qualifier submodule are post-processed based on the *DBCTL* register settings. Furthermore, the delay times are programmable by the registers *DBRED* and *DBFED* for the rising and falling edge delays, respectively. The structure of the *DBCTL* register is shown in the following block diagram.



DBCTL Register Configuration

The submodule register cells allow for the following settings:

- *HALFCYCLE* - Delay counters increment with half TB-counter clock period
- *DEDB_MODE* - Apply falling and rising edge delays to input signal
- *OUTSWAP* - Swap output one or both signals
- *LOADFEDMODE* - Determine when to load DBFED register from shadow to active register
- *LOADREDMODE* - Determine when to load DBRED register from shadow to active register
- *IN_MODE* - Choose source for delay counters; can also be used for output switching
- *POL_SEL* - Invert output polarity
- *OUT_MODE* - Enables Dead-Band bypassing for both outputs

DBFED and *DBRED* are loaded to the active register from the shadow register on the events selected by *LOADFEDMODE* and *LOADREDMODE* bits, respectively. Only shadow mode operation is supported in the PLECS type 4 ePWM module.

In addition to the classic operation available on the type 1 ePWM module, the type 4 ePWM module provides additional operating modes. Refer to [4] for detailed information regarding the configuration of the *DBCTL* register and the additional operating modes.

Mode Description	DBCTL[DEDB-MODE]	DBCTL[OUTSWAP]	
	S8	S6	S7
EPWMxA and EPWMxB signals are as defined by OUT-MODE bits.	0	0	0
EPWMxA = A-path as defined by OUT-MODE bits. EPWMxB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A-signal path)	0	0	1
EPWMxA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B-signal path) EPWMxB = B-path as defined by OUT-MODE bits	0	1	0
EPWMxA = B-path as defined by OUT-MODE bits (falling edge delay or delay-bypassed B-signal path) EPWMxB = A-path as defined by OUT-MODE bits (rising edge delay or delay-bypassed A-signal path)	0	1	1
Rising edge delay applied to EPWMxA / EPWMxB as selected by S4 switch (IN-MODE bits) on A signal path only. Falling edge delay applied to EPWMxA / EPWMxB as selected by S5 switch (IN-MODE bits) on B signal path only.	0	X	X
Rising edge delay and falling edge delay applied to source selected by S4 switch (IN-MODE bits) and output to B signal path only.(1)	1	X	X

(1) When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA ***or*** OUTSWAP bits such that EPWMxA=Bpath. Otherwise, EPWMxA will be invalid.

Additional deadband operation modes [4]

Example Configuration – Step 4

In the sample configuration, the signal *EPWMB* is selected as the source for both delay counters. Further, both the rising and falling edges of the outputs are delayed by 10 counter clock periods and the polarities are not inverted. The *DBCTL* register therefore should be configured as follows.

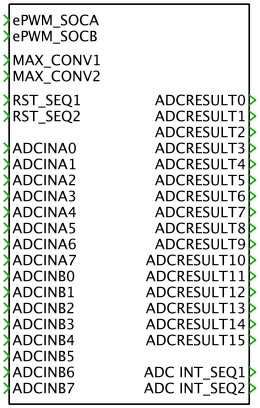
$$DBCTL = 0x0033 \;\hat{=}\; 0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \quad \underbrace{1\,1}_{IN\_MODE} \quad \underbrace{0\,0}_{POL\_SEL} \quad \underbrace{1\,1}_{OUT\_MODE}$$

With the *HALFCYCLE*, *DEDB_MODE*, *OUTSWAP*, *LOADFEDMODE*, and *LOADREDMODE* bits set to zero, the *DBRED* and *DBFED* must be configured to:

$$DBRED = 10 \;\;,\;\; DBFED = 10$$

Analog Digital Converter (ADC) Type 2

The PLECS peripheral library provides two blocks for the TI ADC type 2 module, one with a register based configuration mask and a second with a graphical user interface. The figure below shows the register-based version of the PLECS type 2 ADC module.



Register-based ADC module model

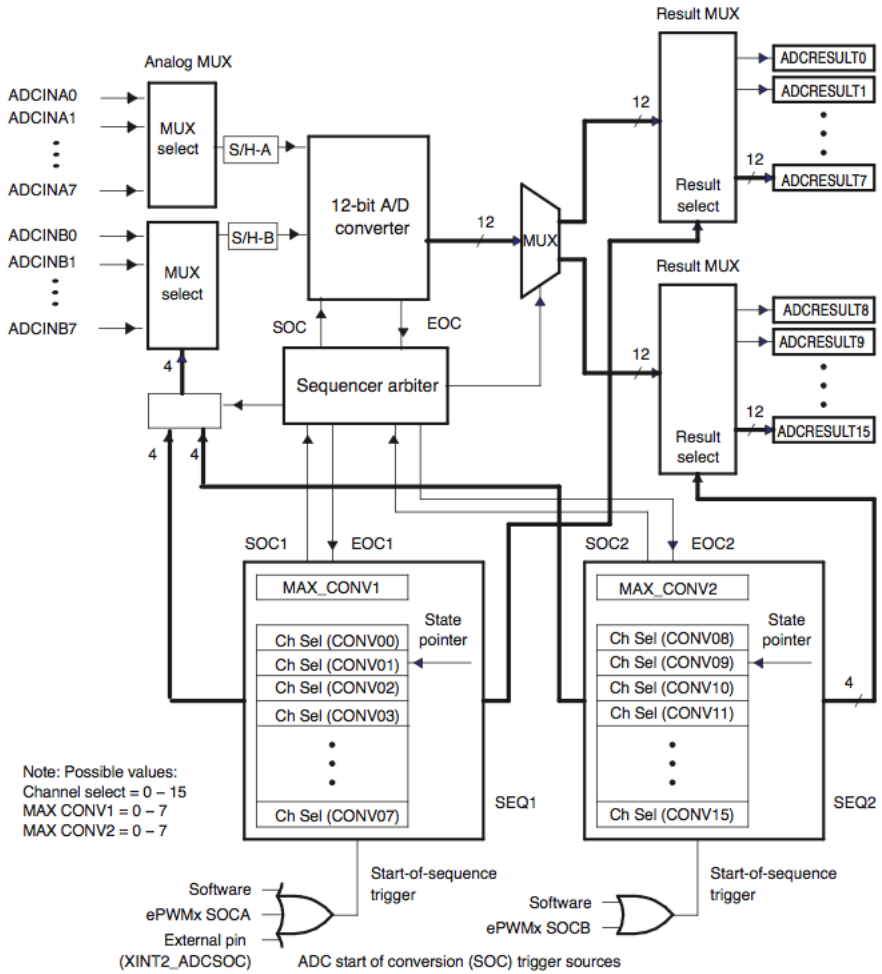
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a graphical user interface to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups:

- *ePWM_SOCx* - input ports to trigger ADC conversions
- *MAX_CONVx* - input ports for number of conversions for sequencers
- *RST_SEQx* - input ports to reset sequencers
- *ADCINA/B* - input ports for measurements
- *ADCRESULTx* - output ports to access conversion results
- *ADC INT_SEQx* - output ports for ADC interrupt triggered at end of sequence of conversions

ADC Module Overview

The PLECS ADC model implements the most relevant features of the MCU peripheral.



Overview of the type 2 ADC module in dual sequencer mode[2]

The ADC model implements the following features:

- ADC Converter with Result Registers

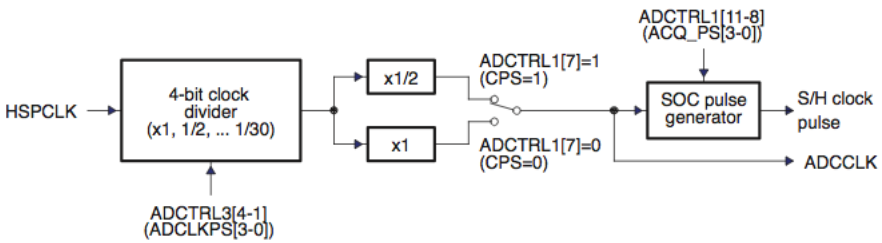
- ADC Sampling Mode
- ADC Sequencer Mode
- ADC Trigger and Interrupt Logic

A section summarizing the differences of the PLECS type 2 ADC module as compared to the actual type 2 ADC module is provided in the “Summary” (on page 81) section.

ADC Converter with Result Registers

The type 2 ADC module contains a single 12-bit converter with dual sample-and-hold (S/H) circuits. The ADC can be configured to perform a series of conversions of preselected input channels each time a start-of-conversion (SOC) request is received. Once a conversion has completed, the result is stored in one of the 16 result registers, *ADCRESULT0 - ADCRESULT15*, as 12 bit unsigned integers. The content of the result registers is available at the output ports of the model.

Note The Output Mode parameter allows the ADC results to be formatted as unsigned integers or quantized doubles.



ADC Core Clock and Sample-and-Hold Clock [2]

The period of the ADC clock, *ADCCLK*, and therefore the time base for the module, is determined based on the peripheral clock, *HSPCLK*, and is scaled down by the *ADCCLKPS*[3:0] bits of the *ADCTRL3* register. An extra clock pre-scaler is provided with the *CPS* bit of the *ADCTRL1* register.

The width of the sampling window in the ADC type 2 is controlled by the *ACQ_PS*[3:0] bits in the *ADCTRL1* register. The ADC sampling time can be

configured to be 1 - 8 cycles of the *ADCCLK* period. The figure above summarizes the scaling of the ADC Core Clock and the S/H clock.

ADC Sampling Mode

The ADC type 2 module can be configured to operate in sequential or simultaneous sampling mode. In the sequential sampling mode the two S/H circuits are operated independently. Any of the 16 input channels can be selected to be sampled by either of the two S/H circuits by configuring the appropriate register bit field *CONVnn* in the *ADCCHSELSEQ1 - ADCCHSELSEQ4* registers. The table below summarizes the input channel configuration using the *CONVnn* bit field in sequential sampling mode.

CONVnn	ADC Input Channel Selected
0000	ADCINA0
0001	ADCINA1
...	...
0111	ADCINA7
1000	ADCINB0
...	...
1111	ADCINB7

In simultaneous sampling mode, the S/H-A circuit can be configured to sample inputs *ADCINA00 - ADCINA07* using the registers bit fields *CONV00 - CONV07*. In this sampling mode, the MSB of *CONVnn* is ignored. The S/H-B circuit will automatically sample the *ADCINBnn* input corresponding to the *ADCINAnn* input that is chosen. For example, if the *CONVnn* register contains the value 0110b, ADCINA6 is sampled by S/H-A and ADCINB6 is sampled by S/H-B. If the value is 1001b, *ADCINA1* is sampled by S/H-A and *ADCINB1* is sampled by S/H-B.

The voltage in S/H-A is converted first, followed by the S/H-B voltage. The result of the S/H-A conversion is placed in the current *ADCRESULTn* register (e.g. *ADCRESULT0*). The result of the S/H-B conversion is placed in the next *ADCRESULTn* register (e.g. *ADCRESULT1*). The next conversion will be placed in the subsequent register (*ADCRESULT2*). The table above summarizes the input channel configuration given by *CONVnn*.

CONVnn	Input pair
0000	ADCINA0 / ADCINB0
0001	ADCINA1 / ADCINB0
...	...
0111	ADCINA7 / ADCINB7
1000	ADCINA0 / ADCINB0
...	...
1111	ADCINA7 / ADCINB7

ADC Sequencer Mode

The ADC module consists of two 8-state sequencers (*SEQ1* and *SEQ2*) that can be operated independently in dual-sequencing mode or can be combined to form one 16-state sequencer (*SEQ1*) in cascaded-sequencing mode. In dual-sequencing mode the maximum number of conversions for *SEQ1* is set by *MAX_CONV1*[2:0] and *SEQ2* by *MAX_CONV2*[2:0] bits in the *ADCMAXCONV* register. Cascaded-sequencing mode can be viewed as *SEQ1* with 16 states instead of 8 where the maximum number of conversions is governed by *MAX_CONV1*[3:0] in the *ADCMAXCONV* register.

Note In the PLECS ADC type 2 module, *MAX_CONV1* and *MAX_CONV2* are inputs that are sampled at SOC trigger events. Both inputs are sampled at trigger events *ePWM_SOCA* and *ePWM_SOCB*.

In the type 2 ADC, SOC requests received during an active sequence remain pending. Pending SOC requests are fulfilled as soon as the sequencer is initiated or immediately after an active sequence of conversions is finished. Additionally, in dual-sequencing mode, an *SEQ1* conversion request is given higher priority over an *SEQ2* conversion request. For example, assume that the converter is busy handling *SEQ1* when an SOC request from *SEQ2* occurs. The converter will start *SEQ2* immediately after completing the active sequence of conversions. If another SOC conversion request from *SEQ2* occurs before the active sequence of conversion is finished, this additional SOC request for

SEQ2 is lost. However, if an SOC request for *SEQ1* is received before the active sequence of conversion is finished, then both SOC requests from *SEQ1* and *SEQ2* will remain pending. When the current *SEQ1* completes its active sequence, the SOC request for *SEQ1* will be taken up immediately. The SOC request for *SEQ2* will remain pending.

The *CONVnn* bit field in the *ADCCHSELSEQ1 - ADCCHSELSEQ4* registers and the sampling mode, define the input pin to be sampled and converted for the result register *ADCRESULTnn*. For further details of the two different sampling modes and the conversion channel configuration, see section "ADC Sampling Mode" (on page 77). The table below summarizes the sequencer differences in the two sequencer modes. Details of the SOC trigger configuration and the ADC interrupt configuration is discussed in section "ADC Interrupt Logic" (on page 80).

Feature	**Single 8-state sequencer 1**	**Single 8-state sequencer 2**	**Cascaded 16-state sequencer**
SOC triggers	ePWM SOCA	ePWM SOCB	ePWM SOCA, ePWM SOCB
Maximum number of auto conversions	8	8	16
Autostop at end-of-sequence	Yes	Yes	Yes
Arbitration Priority	High	Low	Not applicable
ADCCHSELSEQn bit field assignment	CONV00 to CONV07	CONV08 to CONV15	CONV00 to CONV15

In the PLECS ADC type 2 module, sequencer reset can be provided externally by the user. The inputs *RST_SEQ1* and *RST_SEQ2* are used to immediately reset the sequencers, SEQ1 and SEQ2, respectively. At a reset event, the ADC module will fulfill the request of any pending SOC request. If no SOC requests are pending the ADC module remains in idle mode until the next SOC trigger is received. For example, assume that the converter is busy handling *SEQ1* with pending triggers for *SEQ1* and *SEQ2*. If a sequencer 1 reset is received during the conversion, the active conversion is immediately stopped. After the reset, the converter is reinitialized by resetting the state pointer to *CONV00* and the conversion result pointer to *ADCRESULT0*. Once the reinitialization process is completed, the pending *SEQ1* trigger is cleared and the pending *SEQ1* conversion is started. However, if a sequencer 2 reset

is received during the conversion, the SEQ1 conversion is not stopped immediately. The sequencer 2 reset would ensure that the *SEQ2* state pointer is reset to *CONV08* and the conversion result pointer to *ADCRESULT8* when the next SEQ2 conversion occurs.

Additionally, the PLECS ADC type 2 module can be configured to reset the sequencers internally at every or every other end-of-sequence. In this mode, the inputs *RST_SEQ1* and *RST_SEQ2* are ignored. The sequencer cannot be halted in mid sequence and must wait until an end-of-sequence (EOS) event for the next series of conversions to start. An internal reset event at every end-of-sequence would cause the state pointer to reset to *CONV00* and the conversion result pointer to *ADCRESULT0* for SEQ1 after one series of conversions. An internal reset event at every other end-of-sequence would cause the state pointer to reset to *CONV00* and the conversion result pointer to *ADCRESULT0* for *SEQ1* after two series of conversions. After the first series of conversion is completed the state pointer and conversion result pointer are stored. The next set of conversions for SEQ1 will be started from the stored state pointer and conversion result pointer. For example, if the module is configured in simultaneous sampling mode with maximum number of conversions for *SEQ1* set to two conversions, after the first series of conversions the state pointer points to *CONV02* and the conversion result pointer to *ADCRESULT4*. The next conversion of SEQ1 will convert the channel selected in *CONV02* and write the result into *ADCRESULT4*. At the end of the second series of conversions the state pointer is reset to *CONV00* and the conversion result is reset to *ADCRESULT0*.

ADC Trigger and Interrupt Logic

The ADC control register, *ADCTRL2*, can be used to configure the SOC trigger pulses to start a sequence of conversions. In dual-sequencing mode, the *ePWM_SOCB_SEQ2* bit is used to control the start of sequencing of *SEQ2* by an ePWM_SOCB trigger.

- 0 - *SEQ2* cannot be started by ePWM_SOCB trigger
- 1 - *SEQ2* can be started by ePWM_SOCB trigger

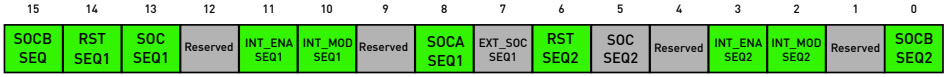
The *ePWM_SOCA_SEQ1* bit is used to control the start of sequencing of *SEQ1* by an ePWM_SOCA signal for both dual-sequencing and cascaded-sequencing modes.

- 0 - *SEQ1* cannot be started by ePWM_SOCA trigger
- 1 - *SEQ1* can be started by ePWM_SOCA trigger

Additionally, in cascaded-sequencing mode the *ePWM_SOCB_SEQ1* bit is used to control the start of sequencing of *SEQ1* by an ePWM_SOCB signal (*SEQ2* is unused in cascaded-sequencing mode).

- 0 - *SEQ1* cannot be started by ePWM_SOCB trigger
- 1 - *SEQ1* can be started by ePWM_SOCB trigger

After every sequence of conversions, the ADC generates an *EOS* pulse with the duration of one ADC clock period. The *ADCTRL2* register can be used to configure the interrupts generated at the end of sequence of *SEQ1* and *SEQ2*. The *INT_ENA_SEQ1* and *INT_ENA_SEQ2* bits are used to control the generation of an ADC interrupt signal for *SEQ1* and *SEQ2*, respectively. With the register below, the interrupt behavior can be configured.



ADC Control Register for ADC trigger and interrupt configuration [2]

The *INT_ENA_SEQx* bit enables the interrupt generation for SEQx.

- 0 - *ADC INT_SEQx* disabled
- 1 - *ADC INT_SEQx* enabled

The *INT_MOD_SEQx* bit configures the generation of an interrupt signal for SEQx at every EOS or every other EOS.

- 0 - ADC interrupt generated for every EOS of SEQx
- 1 - ADC interrupt generated for every other EOS of SEQx

Summary of PLECS Implementation

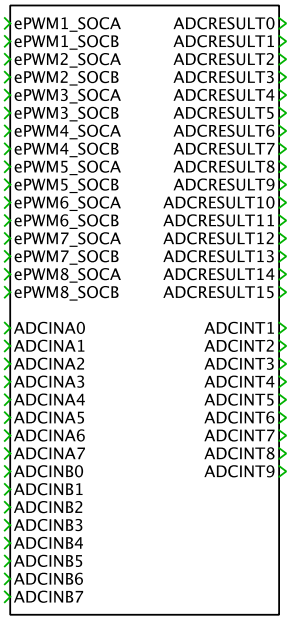
The PLECS type 2 ADC module models the major functionality of the actual TI type 2 ADC module. Below is a summary of differences of the PLECS type 2 ADC module as compared to the actual type 2 ADC module:

- The high and low reference voltages are provided as user inputs on the block mask. The reference voltages must be non-negative and the high reference voltage must be greater than the low reference voltage.
- Both *MAX_CONV1* and *MAX_CONV2* inputs are sampled at trigger events *ePWM_SOCA* and *ePWM_SOCB*.
- Continuous run mode is not supported.
- Sequencer override is not supported.

- Internal sequencer reset at every end-of-sequence or every other end-of-sequence has been modeled for ease of use. See section “ADC Sequencer Mode” (on page 78) for more details.
- The output results are provided either as unsigned integers (right justified) or as quantized double values.

Analog Digital Converter (ADC) Type 3

The PLECS peripheral library provides two blocks for the TI ADC type 3 module, one with a register based configuration mask and a second with a graphical user interface. The figure below shows the appearance of the block.



ADC module model

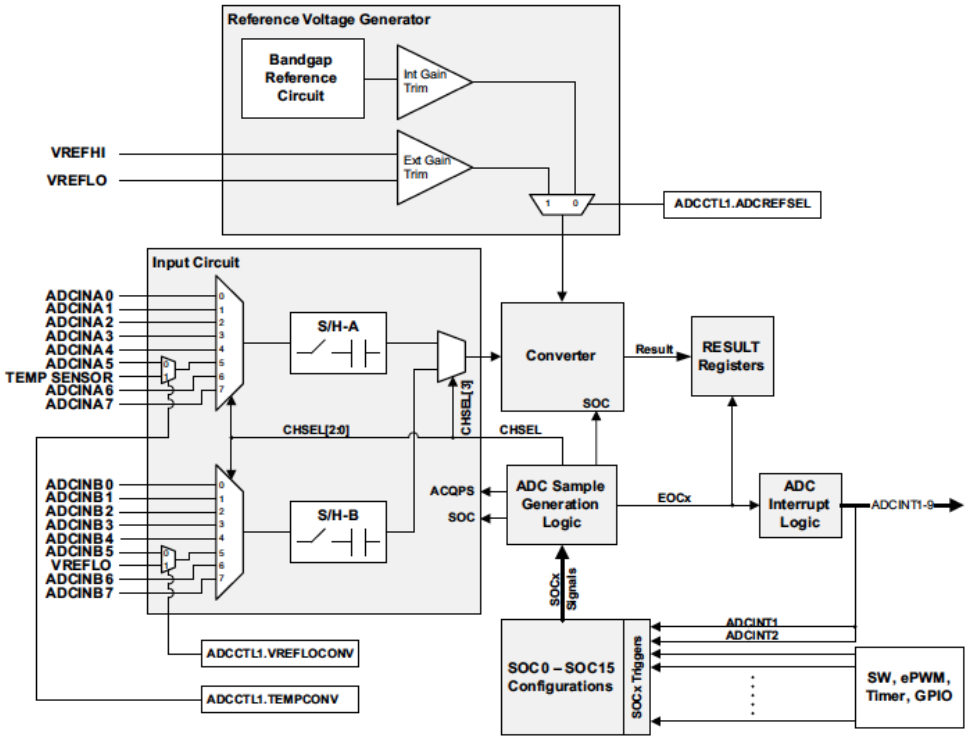
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a graphical user interface to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *ePWMx_SOCy* - input ports to trigger ADC conversions
- *ADCINA/B* - input ports for measurements
- *ADCRESULTx* - output ports to access conversion results
- *ADCINTx* - output ports for subsequent logic triggered by a conversion end

ADC Module Overview

The PLECS ADC model implements the most relevant features of the MCU peripheral.



Overview of the type 3 ADC module [1]

The ADC model implements these logical submodules:

- ADC Converter with Result Registers
- ADC Reference Voltage Generator
- ADC Sample Generation Logic
- ADC Input Circuit
- ADC Interrupt Logic

ADC Converter with Result Registers

The type 3 ADC module contains a single 12-bit converter. Either an internal or an external voltage reference can be selected.

The converter takes 13 ADC clocks for a single conversion. The period of the ADC clock, and therefore the time base for the module, is determined based on the system clock and the two clock dividers specified in the *ADCCTL2* register.

ADCCTL2 Register structure

By using the bits *CLKDIV4EN* and *CLKDIV2EN* the ADC time base can be specified as follows.

CLKDIV2EN	CLKDIV4EN	ADC clock
0	0	SYSCLK
0	1	SYSCLK
1	0	SYSCLK / 2
1	1	SYSCLK / 4

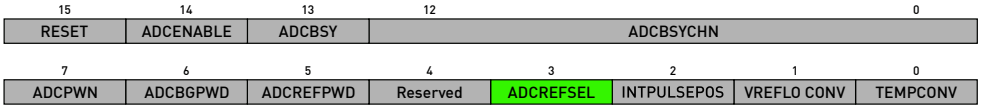
The bit *ADCNONOVERLAP* determines if an overlap of sampling and conversion is allowed in case of multiple pending conversion requests.

- 0 - Overlap is allowed
- 1 - Overlap is not allowed

Once a conversion has completed, the result is stored to one of the 16 result registers *ADCRESULT0 - ADCRESULT15*. These are directly associated with the *SOC*. The content of the result registers is available at the output ports of the model. The representation of the conversion result can be chosen with the mask parameter **Output Mode**.

ADC Reference Voltage Generator

The ADC can use an internal or an external reference voltage. The internal bandgap range is *[0V...3.3V]*, while the external reference can be specified in the component mask.



ADCCTL1 Register structure

With the bit *ADCREFSEL*, the desired voltage reference can be chosen.

- 0 - Internal bandgap
- 1 - Reference voltages defined by module mask

The component only supports the late interrupt pulse mode. Therefore the bit *INTPULSEPOS* should be one.

ADC Sample Generation Logic

The ADC Sample Generation Logic responds to the *SOCx* signals, which are based on 16 individual sets of configuration parameters *SOC0 - SOC15*. Every *SOC* contains the following information:

- Size of Sampling Window (*ACQPS*)
- Converted Input Channel (*CHSEL*)
- Trigger Signal (*TRIGSEL*)

The register used for configuring a *SOC* is shown below.

ADCSOCxCTL Register structure

The register cell *ACQPS* defines the length of the sampling window. The minimum value valid is 06_h which sets the Sample Window to 6+1 ADC clock cycles. Note according to the hardware documentation, there are a number of invalid settings for this register field:

$$10_h\ ,\ 11_h\ ,\ 12_h\ ,\ 13_h\ ,\ 14_h\ ,\ 1D_h\ ,\ 1E_h\ ,\ 1F_h\ ,\ 20_h\ ,\ 21_h\ ,\ 2A_h\ ,\ 2B_h\ ,\ 2C_h$$

$$2D_h\ ,\ 2E_h\ ,\ 37_h\ ,\ 38_h\ ,\ 39_h\ ,\ 3A_h\ ,\ 3B_h$$

The time needed for a full conversion can be calculated with the following equation.

$$T_{conv} = \underbrace{(ACQPS + 1) \cdot ADC_{clk}}_{Sampling Window} + \underbrace{13 \cdot ADC_{clk}}_{Conversion}$$

The *CHSEL* field associates an input pin with a specific *SOC*. The component allows single and simultaneous sampling – see section "ADC Input Circuit" (on page 89). For a *SOC* in single sample mode, cell configuration is as follows.

CHSEL	Input
0h	ADCINA0
1h	ADCINA1
...	...
7h	ADCINA7
8h	ADCINB0
...	...
Fh	ADCINB7

In case of simultaneous sample mode, the channel selection is configured as pairs.

CHSEL	Input pair
0h	ADCINA0 / ADCINB0
1h	ADCINA1 / ADCINB0
...	...
7h	ADCINA7 / ADCINB7
> 7h	Invalid Selection

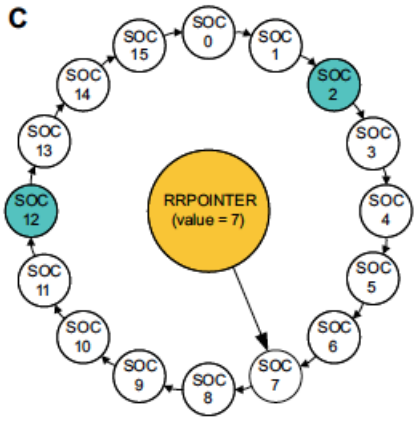
With the *TRIGSEL* field it is possible to choose a particular trigger source available as a block input. The PLECS component only supports *ePWMx_SOCy* trigger signals. The following table shows the mapping to the hexadecimal representation. Configurations above 14_h and below 05_h are invalid and result in an error.

Additionally, it is possible to configure the interrupt signals *INT1* and *INT2* to trigger ADC conversions. See section "ADC Interrupt Logic" (on page 90) for further details.

During operation of an ADC, more than one conversion trigger can occur simultaneously. A *SOC* can also be triggered while a conversion is already ac-

TRIGSEL	Input / Source
05h	ePWM1_SOCA
06h	ePWM1_SOCB
07h	ePWM2_SOCA
...	...
14h	ePWM8_SOCB

tive. A round robin method prioritizes pending *SOCs*. This scheme is accurately reflected by the PLECS component. The figure below shows an example snapshot of the round robin wheel.



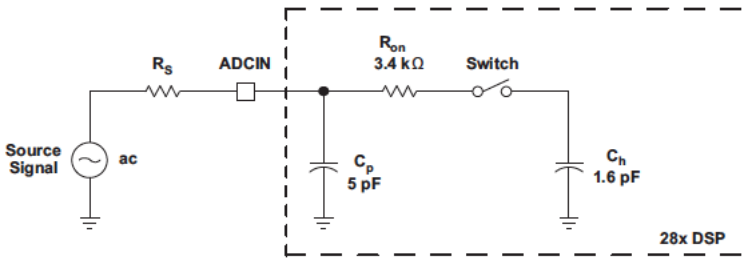
ADC Prioritization example [1]

This wheel consist of 16 *SOC* flags and a round robin pointer (*RRPOINTER*). A *SOC* flag is set when a trigger is received and is cleared when the corresponding conversion finishes. The round robin pointer always points to the last converted *SOC* and is changed with the end of every conversion. In the PLECS ADC model, the round robin pointer initially points to *SOC15*. In the example above, the round robin pointer points to *SOC7* indicating this is the last converted *SOC*. At this point in time, the *SOC2* and *SOC12* are triggered and the corresponding flags are set. For prioritization, the ADC starts with RRPOINTER+1 and goes clockwise through the round robin wheel, meaning *SOC12* is executed next in this example.

The hardware ADC also provides higher prioritized *SOCs* and a *ONESHOT* single conversion mode. These are not supported by the PLECS model.

ADC Input Circuit

The Input Circuit of the type 3 ADC module consists of two separate Sample&Hold circuits (S&H), each connected to a multiplexer. The field *CHSEL* from the *ADCSOCxCTL* register associates an input with a particular *SOC*. Measurements of *TEMP SENSOR* and *VREFLO* are not supported by the PLECS model. The figure below shows the hardware circuit schematic of an *ADCIN* voltage connected to an S&H circuit.



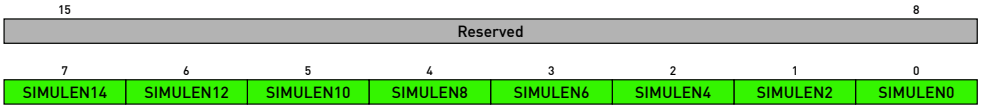
ADCInx Input Model [1]

After an *SOC* is triggered from the round robin wheel, the switch is closed for the sampling window changing the voltage of the sampling Capacitor C_h. Once the sampling time has elapsed, the switch is opened and the conversion starts. For simulation efficiency reasons, the PLECS model of the ADC approximates this behavior by taking the average of the input values at the begin and end of the sampling window.

The type 3 ADC further provides single as well as simultaneous measurements. For a single measurement, only one S&H circuit is active at a time. For simultaneous measurements, both S&H circuits operate in parallel, sampling two different voltages at the same time. The conversion is carried out sequentially starting with the upper S&H voltage. The sampling mode is assigned pairwise, always in groups of even and odd *SOCs* using the register shown below.

With the bit *SIMULENx*, the sampling mode can be chosen as follows.

- 0 - Single sample mode for *SOCx* and *SOCx+1*
- 1 - Simultaneous sample mode set for *SOCx* and *SOCx+1*



ADCSAMPLEMODE Register structure

In case of simultaneous mode, both *SOCs* can still be configured independently by the *ADCSOCxCTL* registers. The behavior during conversion (sample window length and channel selection) is always determined by the triggered *SOC*. For a more advanced understanding of the modules behavior and configuration, please refer to [1].

ADC Interrupt Logic

For every conversion, the ADC sample generation logic generates an end of conversion pulse (*EOC*) with duration one ADC clock period. This pulse is generated one cycle before latching the conversion result. The interrupt pulse always lags the *EOC* pulse by one ADC clock period and therefore is simultaneous to the result latch. The ADC Interrupt Logic can generate the interrupts *ADCINT1-ADCINT9*, which are available at the output ports of the ADC model. With the register below, the interrupt behavior can be configured.

INTSELxNy Register structure for the example of INT1 and INT2

The *INTxE* bit enables the interrupt generation by an *EOC* flag.

- 0 - *ADCINTx* disabled
- 1 - *ADCINTx* enabled

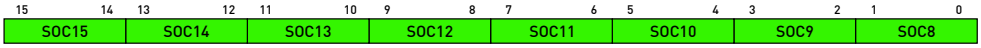
The *INTxSEL* cell defines which *EOC* flag triggers the interrupt.

INTxSEL	Interrupt Trigger
00h	EOC0 triggers interrupt ADCINTx
01h	EOC1 triggers interrupt ADCINTx
...	...
0Fh	EOC15 triggers interrupt ADCINTx
> 0Fh	Invalid Selection

Note The cells *INT10E* and *INT10SEL* in *INTSEL9N10* have no effect because the model only supports the interrupts *ADCINT1-ADCINT9*.

Additionally, the interrupts *INT1* and *INT2* can be configured to internally trigger *SOCs*, using the the following registers:

ADCINTSOCSEL1 Register structure



ADCINTSOCSEL2 Register structure

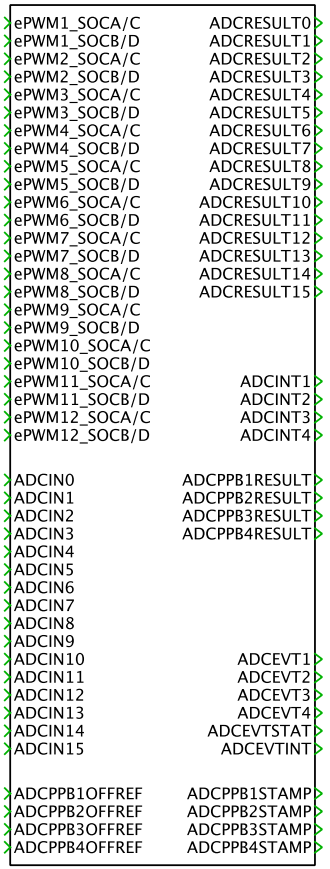
The field *SOCx* can be configured as follows.

SOCx	Interrupt Trigger
00	No ADCINT will trigger SOCx
01	ADCINT1 will trigger SOCx
10	ADCINT2 will trigger SOCx
11	Invalid Selection

The setting in this register, if not 00, overwrites the trigger setting defined in the field *TRIGSEL* of the *ADCSOCCTLx* register.

Analog Digital Converter (ADC) Type 4

The PLECS peripheral library provides two blocks for the TI ADC type 4 module, one with a register based configuration mask and a second with a graphical user interface. The figure below shows the appearance of the block.



ADC module model

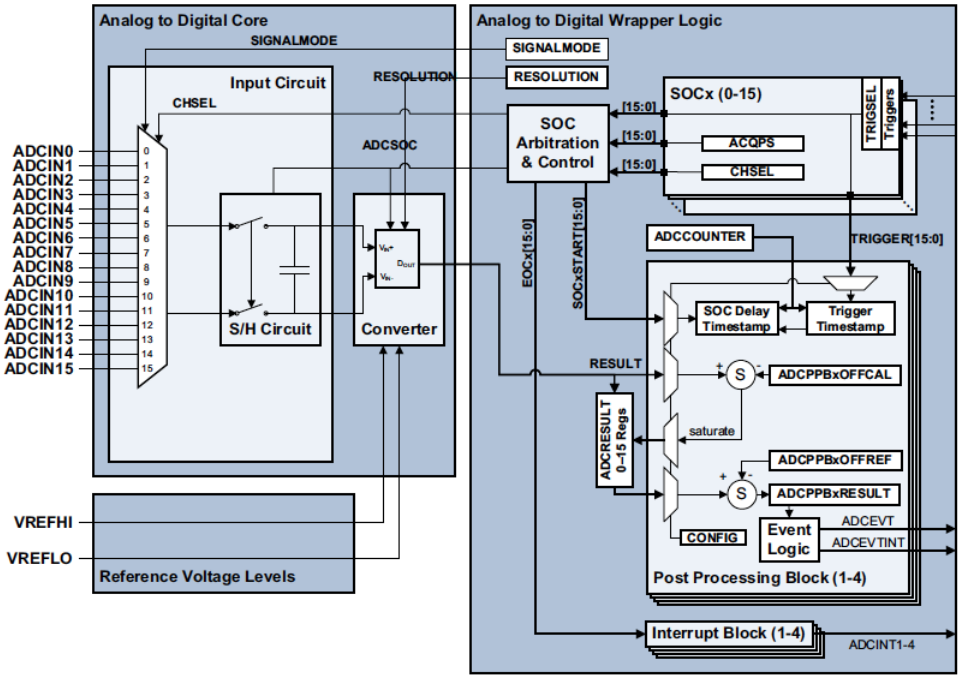
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a graphical user interface to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *ePWMx_SOCy/z* - input ports to trigger ADC conversions
- *ADCINx* - input ports for measurements
- *ADCPPBxOFFREF* - input ports for PPB error calculation
- *ADCRESULTx* - output ports to access conversion results
- *ADCINTx* - output ports for subsequent logic triggered by a conversion end
- *ADCPPBxRESULT* - output ports to access PPB results
- *ADCEVTx* - output ports for PPB events
- *ADCEVTSTAT* - access to PPB event status register
- *ADCEVTINT* - output ports for PPB interrupts
- *ADCPPBxSTAMP* - output ports to access PPB DLYSTAMP

ADC Module Overview

The PLECS ADC model implements the most relevant features of the MCU peripheral.



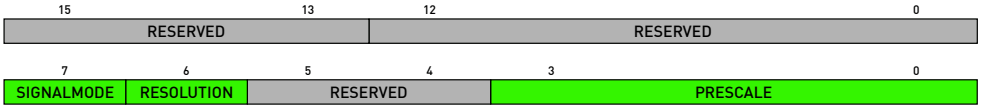
Overview of the type 4 ADC module [4]

The ADC model implements these logical submodules:

- AD Core with Input Circuit and Converter and Result Register
- AD Wrapper with SOC Arbitration & Control and Interrupt Block
- ADC Post-Processing Blocks

ADC Converter and Result Register

The type 4 ADC module contains a single converter with an external voltage reference specified in the component mask. It supports 12-bit and 16-bit resolution and can be operated in single-ended or differential mode depending on the settings in the *ADCCTL2* register.



ADCCTL2 Register structure

The bits *SIGNALMODE* and *RESOLUTION* determine the behavior and the resolution used by the ADC. Please note that only the following combinations are valid:

SIGNALMODE/RESOLUTION	12-bit (0)	16-bit (1)
Single-Ended (0)	x	
Differential (1)		x

The converter takes 29.5 (16-bit) or 10.5 (12-bit) ADC clocks for a single conversion. The period of the ADC clock is derived from the system clock, specified in the component mask, and the *PRESCALE* bit specified in the *ADCCTL2* register.

PRESCALE	ADC Clock
0h	ADCCLK = System Clock / 1.0
1h	Invalid
2h	ADCCLK = System Clock / 2.0
3h	ADCCLK = System Clock / 2.5
4h	ADCCLK = System Clock / 3.0
...	...
Fh	ADCCLK = System Clock / 8.5

Once a conversion has completed, the result is stored to one of the 16 result registers *ADCRESULT0 - ADCRESULT15*. These are directly associated with the *SOC*. The content of the result registers is available at the output ports of the model. The representation of the conversion result can be chosen with the mask parameter **Output Mode**.

ADC SOC Arbitration & Control

The ADC Arbitration Logic is defined by *SOCx* configurations, which consist of 16 individual sets of configuration parameters *SOC0 - SOC15*. Every *SOC* contains the following information:

- Size of Sampling Window (*ACQPS*)
- Converted Input Channel (*CHSEL*)
- Trigger Signal (*TRIGSEL*)

The register used for configuring a *SOC* is shown below.

ADCSOCxCTL Register structure

The register cell *ACQPS* defines the length of the sampling window. The sampling window is determined by the system clock and needs to be chosen to last at least one ADC clock period.

The time needed for a full single ended conversion can be calculated as follows.

$$T_{conv\_single-ended} = \underbrace{(ACQPS + 1) \cdot SYS_{clk}}_{Sampling Window} + \underbrace{10.5 \cdot ADC_{clk}}_{Conversion}$$

For a differential conversion, the time needed is determined by

$$T_{conv\_differential} = \underbrace{(ACQPS + 1) \cdot SYS_{clk}}_{Sampling Window} + \underbrace{29.5 \cdot ADC_{clk}}_{Conversion}$$

The *CHSEL* field associates an input (single-ended mode) or a pair of inputs (differential mode) with a specific *SOC*. For more details, see section "ADC Input Circuit" (on page 99). In single-ended mode, the input configuration for a *SOC* is as follows.

CHSEL	Input
0h	ADCIN0
1h	ADCIN1
...	...
Fh	ADCIN15

In case of differential mode, the channel selection is configured as pairs.

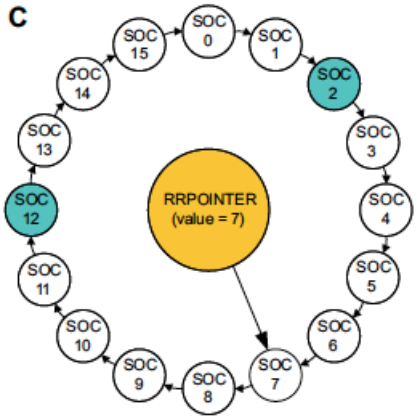
CHSEL	Input pair
0h	ADCIN0 / ADCIN1
1h	ADCIN0 / ADCIN1
2h	ADCIN2 / ADCIN3
3h	ADCIN2 / ADCIN3
...	...
Eh	ADCIN14 / ADCIN15
Fh	ADCIN14 / ADCIN15

With the *TRIGSEL* field it is possible to choose a particular trigger source available as a block input. The ADC model only supports *ePWMx_SOCy/z* trigger signals. The following table shows the mapping to the hexadecimal representation. Configurations above $1C_h$ and below 05_h are invalid and result in an error.

TRIGSEL	Input / Source
05h	ePWM1_SOCA/C
06h	ePWM1_SOCB/D
07h	ePWM2_SOCA/C
08h	ePWM2_SOCB/D
...	...
1Bh	ePWM8_SOCA/C
1Ch	ePWM8_SOCB/D

Additionally, it is possible to configure the interrupt signals *INT1* and *INT2* to trigger ADC conversions. See section “ADC Interrupt Logic” (on page 100) for further details.

During operation of an ADC, more than one conversion trigger can occur simultaneously. A *SOC* can also be triggered while a conversion is already active. A round robin method prioritizes pending *SOCs*. This scheme is accurately reflected by the PLECS component. The figure below shows an example snapshot of the round robin wheel.



ADC Prioritization example [4]

This wheel consist of 16 *SOC* flags and a round robin pointer (*RRPOINTER*). A *SOC* flag is set when a trigger is received and is cleared when the corre-

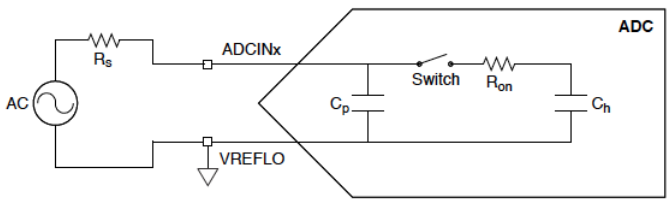
sponding conversion finishes. The round robin pointer always points to the last converted *SOC* and is changed with the end of every conversion. In the PLECS ADC model, the round robin pointer initially points to *SOC15*. In the example above, the round robin pointer points to *SOC7* indicating this is the last converted *SOC*. At this point in time, the *SOC2* and *SOC12* are triggered and the corresponding flags are set. For prioritization, the ADC starts with RRPOINTER+1 and goes clockwise through the round robin wheel, meaning *SOC12* is executed next in this example.

The hardware ADC also provides higher prioritized *SOCs*, software triggering and a *burst* mode. These are not supported by the PLECS model.

ADC Input Circuit

The Input Circuit of the type 4 ADC module consists of a single Sample&Hold circuit (S&H) connected to a multiplexer.

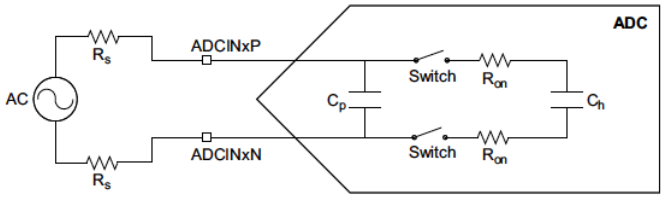
In single-ended mode, a single input is connected to the S&H circuit as shown below.



ADCInx Input Model in Single-Ended Mode [4]

In this mode, a single input voltage is converted with 12bit resolution. The ADC operates in range [VREFLO ... VREFHI]. The reference voltage can be specified in the component mask.

In differential mode, the difference between two voltages can be measured with 16-bit resolution.



ADCInx Input Model in Differential Mode [4]

In this mode, the ADC operates in range [-VREFHI ... VREFHI].

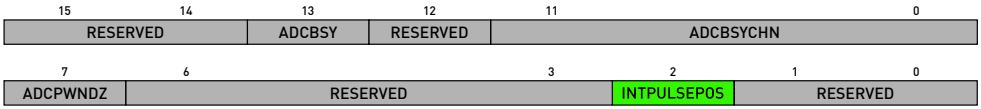
The field *CHSEL* from the *ADCSOCxCTL* register associates an input or a pair of inputs with a particular *SOC*.

After an *SOC* is triggered from the round robin wheel, the switch is closed for the sampling window changing the voltage of the sampling Capacitor C_h. Once the sampling time has elapsed, the switch is opened and the conversion starts. For simulation efficiency reasons, the PLECS model of the ADC approximates this behavior by taking the average of the input values at the begin and end of the sampling window.

The behavior during conversion (sample window length and channel selection) is always determined by the triggered *SOC*. For a more advanced understanding of the modules behavior and configuration, please refer to [4].

ADC Interrupt Logic

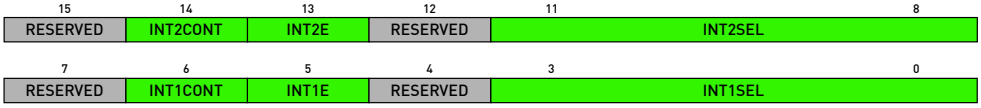
For every conversion, the SOC Arbiter logic generates an end of conversion pulse (*EOC*). This pulse results in an interrupt pulse with duration of one system clock. The component only supports the late interrupt pulse mode. Therefore the bit *INTPULSEPOS* in the *ADCCTL1* register needs to be set to one.



ADCCTL1 Register structure

Based on this, the interrupt pulses always occur synchronous to latching the conversion results to the output.

The ADC Interrupt Logic can generate the interrupts *ADCINT1-ADCINT4*, which are available at the output ports of the ADC model. With the register below, the interrupt behavior for *INT1* and *INT2* can be configured.



ADCINTSELxNy Register structure for the example of INT1 and INT2

In the model, the Interrupt Logic can only be operated in Continuous Mode. Therefore, the bit *INTxCONT* always needs to be set.

The *INTxE* bit enables the interrupt generation by an *EOC* flag.

- 0 - *ADCINTx* disabled
- 1 - *ADCINTx* enabled

The *INTxSEL* cell defines which *EOC* flag triggers the interrupt.

INTxSEL	Interrupt Trigger
0h	EOC0 triggers interrupt ADCINTx
1h	EOC1 triggers interrupt ADCINTx
...	...
Fh	EOC15 triggers interrupt ADCINTx

Additionally, the interrupts *INT1* and *INT2* can be configured to internally trigger *SOCs*, using the the following registers:

ADCINTSOCSEL1 Register structure

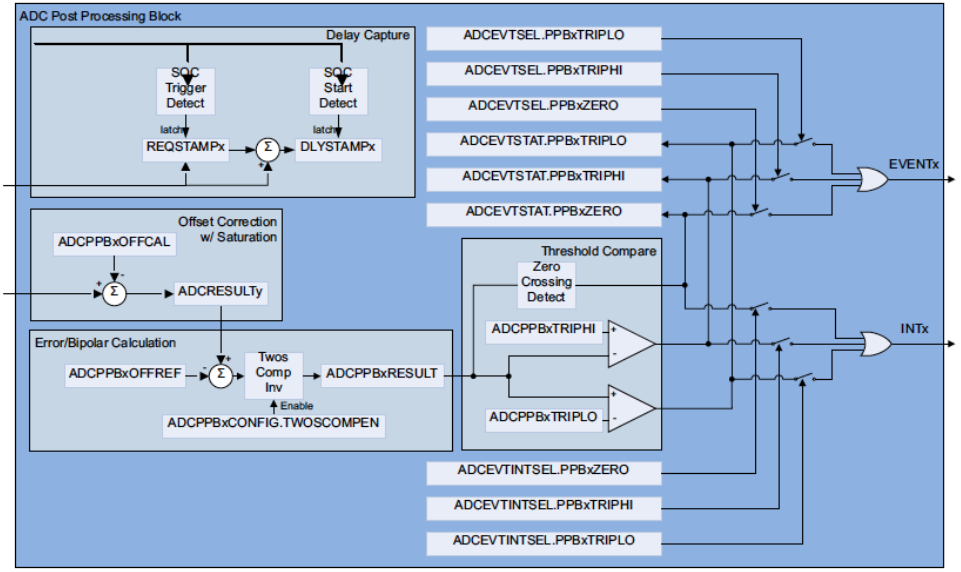
ADCINTSOCSEL2 Register structure

SOCx	Interrupt Trigger
00	No ADCINT will trigger SOCx
01	ADCINT1 will trigger SOCx
10	ADCINT2 will trigger SOCx
11	Invalid Selection

The setting in this register, if not 00, overwrites the trigger setting defined in the field *TRIGSEL* of the *ADCSOCCTLx* register.

Post-Processing Blocks

The type 4 ADC module contains four PPB blocks to post-process the conversion results. The figure below shows the block diagram of a single submodule.

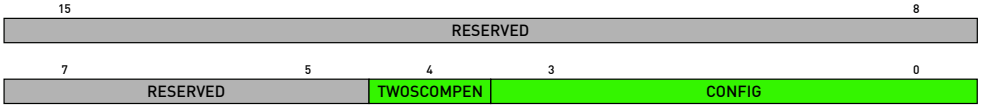


Overview of the type 4 ADC PPB submodule [4]

The PPB blocks add the following features to the ADC.

- PPB Offset Correction
- PPB Error Calculation
- PPB Limit and Zero-Crossing Detection
- PPB Sample Delay Capture

Each PPB block is associated to a single SOC. This can be configured with the register *ADCPPBxCONFIG* shown below.



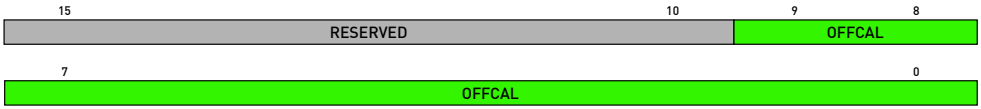
ADCPPBxCONFIG Register structure

The field *CONFIG* determines the associated SOC.

CONFIG	SOC
0h	SOC0
1h	SOC1
...	...
Fh	SOC15

Note that multiple PPB blocks can point to a single SOC. The default used is *SOC0*.

The PPB block implements an offset correction for the conversion result of the associated SOC. The result of this calculation is presented at the *ADCRESULTx* output. The calculation further saturates at 0 at the low end and either 4095 or 65535 at the high end, depending on the signal mode (single-ended or differential). The offset can either be positive or negative and is defined by the *ADCPPBxOFFCAL* register shown below.



ADCPPBxOFFCAL Register structure

The field *OFFCAL* defines the offset used.

OFFCAL	OFFSET
0h	-1
1h	-2
...	...
1FFh	-512
200h	+512
...	...
3FEh	+2
3FFh	+1

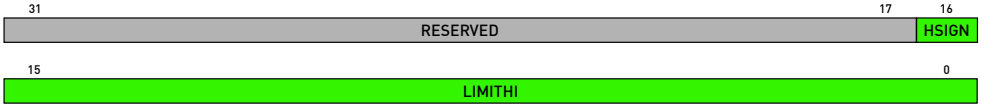
Note If multiple PPB's are associated to an SOC, the *ADCPPBxOFFCAL* register of the PPB with the highest ID is used for the calculation.

In addition to the offset calculation, the PPB implements an error calculation depending on the field *TWOSCOMPEN* in the *PPBxCONFIG* register and the *ADCPPBxOFFREF* input.

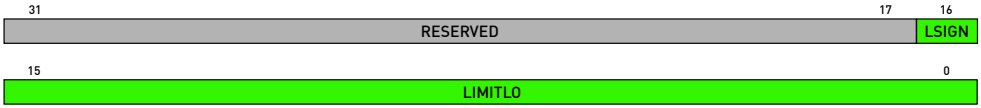
- 0 - *ADCPPBxRESULT* = *ADCRESULTx* - *ADCPPxOFFREF*
- 0 - *ADCPPBxRESULT* = *ADCPPxOFFREF* - *ADCRESULTx*

The result of this calculation produces a sign extended integer result and is available at the *ADCPPBxRESULT* output.

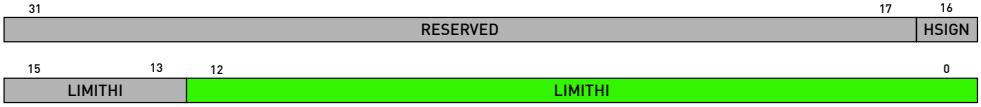
The PPB block further implements a Zero-Crossing- and Limit-Detection for the PPB results. The Limits compared to the *ADCPPBxRESULT* registers are specified with the trip registers shown below.



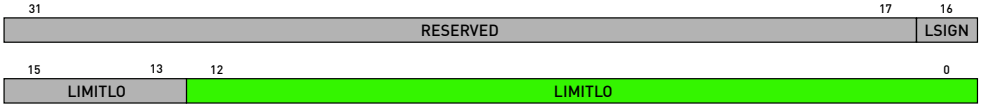
ADCPPBxTRIPHI Register structure for differential mode (16-bit)



ADCPPBxTRIPLO Register structure for differential mode (16-bit)



ADCPPBxTRIPHI Register structure for single-ended mode (12-bit)

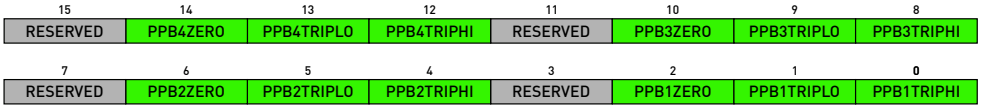


ADCPPBxTRIPLO Register structure for single-ended mode (12-bit)

Please note that the bits used within those registers depend on the signal mode. For the registers *ADCPPBxRESULT*, *ADCPPBxTRIPLO* and *ADCPPBxTRIPHI*, the bit usage is indicated below.

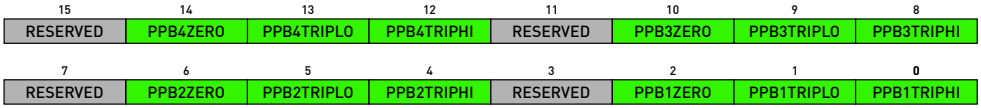
SIGNALMODE	Sign bit	Data bits
0 - single-ended	12	[11:0]
1 - differential	16	[15:0]

The information from the Zero-Crossing- and Limit-Detection is stored within the *ADCEVTSTAT* register.

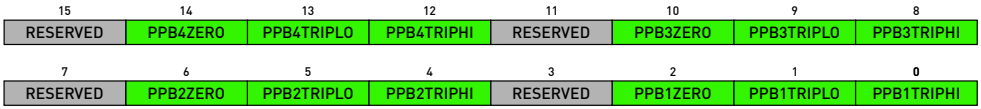


ADCEVTSTAT Register structure

This register is shared by all PPB blocks and is available at the model output. The status can further be used to generate ADC-Events and/or ADC-Interrupts. The state changes resulting in events and interrupts are configured using the *ADCEVTSEL* and *ADCINTEVTSEL* registers in the mask.



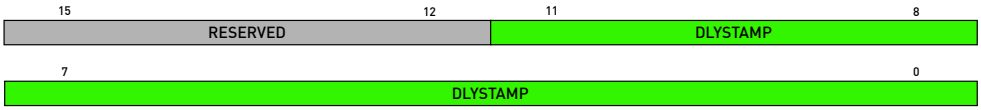
ADCEVTSEL Register structure



ADCINTEVTSEL Register structure

While every PPB hast its own ADCEVTx output, all PPBs share one interrupt flag available at the ADCEVTINT output.

Each PPB further provides a functionality to capture the delay between a trigger to the associated SOC and the effective start of the conversion. This information is provided as multiples of the used system clock period and stored in the *ADCPPBxSTAMP* register.

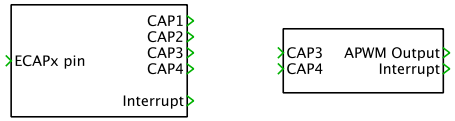


ADCPPBxSTAMP Register structure

Note The DLYSTAMP is calculated based on a 12-bit counter and wraps around at 4095.

Enhanced Capture (eCAP) Type 0

The PLECS peripheral library provides two blocks for the TI eCAP Type 0 module operated in capture mode: one with a register based configuration mask and a second with a graphical user interface (GUI). The peripheral library also includes a block for the TI eCAP Type 0 module operated in APWM mode. The figure below shows the GUI-based version of the PLECS Type 0 eCAP module operated in capture mode and the PLECS Type 0 eCAP module operated in APWM mode.



PLECS eCAP modules operated in APWM and Capture modes

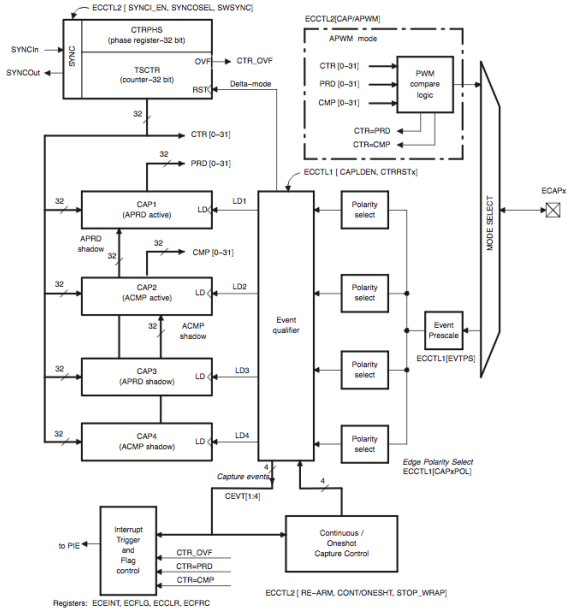
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

The PLECS eCAP models implement the most relevant features of the MCU peripheral.

eCAP Module Operated in Capture Mode

When operated in capture mode, the eCAP module interfaces with other PLECS components over the following terminal groups:

- *ECAPx_pin* - input ports to capture the pulse train
- *CAPx* - output ports to access capture registers 1-4
- *Interrupt* - output port for eCAP interrupt trigger



Overview of the type 0 eCAP module in capture mode [3]

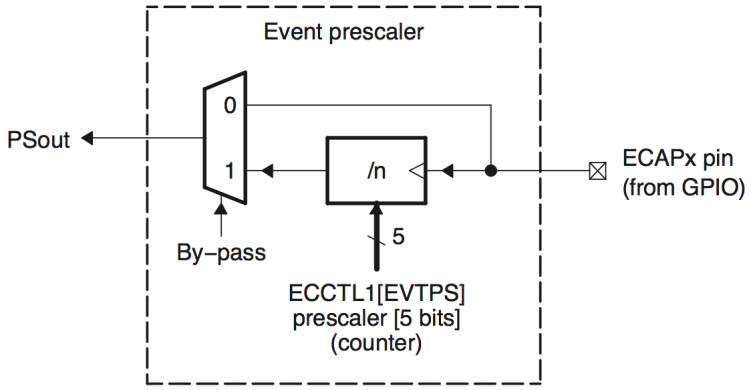
The eCAP model operated in capture mode implements the following features:

- Event Prescaler
- Edge Polarity Select and Capture Control

Event Prescaler

The event prescaler bits *ECCTL1[13:9]* can be used to reduce the frequency of the input capture signal. When a prescale value of 1 is chosen (i.e., *ECCTL1[13:9]* = 0,0,0,0,0) the input capture signal bypasses the prescale logic

completely. Alternatively, the prescaler can be scaled by a factor of 2 to 62 using the *ECCTL1[13:9]* bits. This is useful when very high frequency signals are used as inputs.



Event prescaler control [3]

Edge Polarity Select and Capture Control

Independent edge polarities can be selected for each of the 32-bit *CAP1-4* registers to capture the counter value. Loading of the capture registers can be disabled by clearing the *CAPLDEN* bits in the *ECCTL1* register. The bits *CAPxPOL* in the *ECCTL1* are used to configure the *CAPx* capture event on a rising or falling edge.

The PLECS eCAP module can only be operated in continuous capture control mode. A 2-bit counter continues to run (0->1->2->3->0) and capture values continue to be written to *CAP1-4* in a circular buffer sequence. The *CTRRST1-4* bits in the *ECCTL1* register can be used to force the counter to reset after a capture event. This is useful when the eCAP module is operated in difference mode.

The *STOP_WRAP* bits in the *ECCTL2* register can be used to program the 2-bit counter wrapping to occur after any of the four capture events.

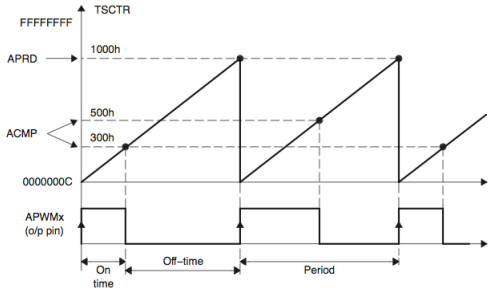
Note The PLECS eCAP module does not support One-Shot capture control mode.

---

eCAP Module Operated in APWM Mode

When operated in APWM mode, the eCAP module interfaces with other PLECS components over the following terminal groups:

- *CAP3* - input port for period shadow register
- *CAP4* - input port for compare shadow register
- *APWM Output* - output port for the APWM gating signal
- *Interrupt* - output port for eCAP interrupt trigger



PWM waveform details of eCAP module operated in APWM mode [3]

The PLECS APWM mode supports shadow mode operation only. The *CAP3-4* register values are transferred to their active register on a period event. The *CAP3* input corresponds to writing to the period shadow register and the *CAP4* input corresponds to writing to the compare shadow register.

Note Immediate update operation in APWM mode is not supported.

---

eCAP Interrupts

In capture mode, the eCAP module can be configured to generate an interrupt at any of the 4 capture events using the *CEVTx* bits in the *ECEINT* register.

In APWM mode, the eCAP module can be configured to generate an interrupt at counter equals period and counter equals compare events. This can be done by setting the *CTR=PRD* and *CTR=CMP* bits in the *ECEINT* register, respectively.

In both modes, a counter overflow event (FFFFFFFF->00000000) can be configured to produce an interrupt by configuring the *CTROVF* bit in the *ECEINT* register.

Note Flags used to generate the interrupt signal are automatically cleared in the PLECS eCAP module after one system clock period for ease of use.

---

eCAP Counter Update

The PLECS eCAP module provides users access to the 32-bit counter as a probe signal. To improve simulation efficiency the counter value is not sampled every system clock period. Instead, the user defines a counter sampling frequency to sample the counter value at the desired frequency.

Note Higher counter sampling frequency increases counter resolution but reduces simulation speed.

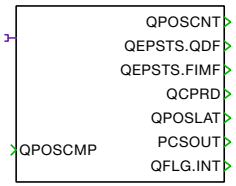
Summary of PLECS Implementation

The PLECS eCAP module models the major functionality of the actual TI type 0 eCAP module. Below is a summary of the differences between the PLECS Type 0 eCAP module and the actual Type 0 eCAP module:

- No delay between capture event and capture value becoming valid.
- One-Shot capture control mode is not supported.
- Immediate update operation in APWM mode is not supported.
- Flags used to generate the interrupt signal are automatically cleared.
- Counter sampling frequency provides user control of the counter resolution. A higher resolution leads to slower simulation speed.

Enhanced Quadrature Encoder Pulse (eQEP) Type 0

The PLECS peripheral library provides two blocks for the TI eQEP type 0 module, one with a register based configuration mask and a second with a graphical user interface (GUI). The figure below shows the register-based version of the PLECS type 0 eQEP module.



Register-based eQEP module

The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

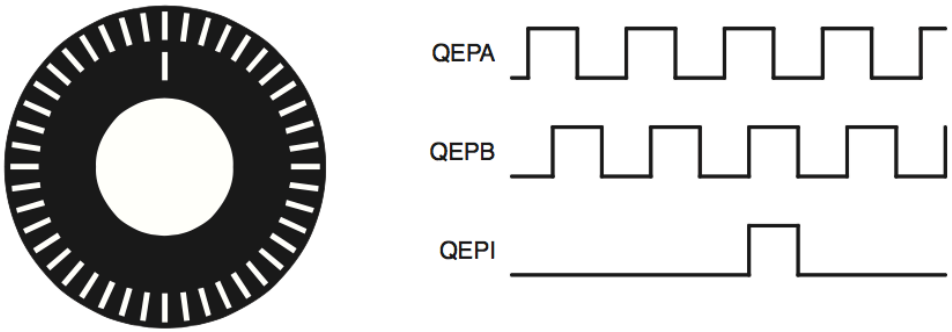
The PLECS eQEP models implement the most relevant features of the MCU peripheral. The eQEP module also incorporates a model of a simplified encoder disk in order to maintain simulation efficiency.

Both eQEP blocks interface with other PLECS components over the following terminal groups:

- *Mechanical Input* - input port to connect the rotor shaft
- *QPOSCMP* - input port for the eQEP position-compare register
- *QPOSCNT* - output port for eQEP counter
- *QEPSTS.QDF* - output port for direction of rotation
- *QEPSTS.FIMF* - output port for first index marker flag
- *QPOSLAT* - output port for eQEP position counter latched register
- *PCSOUT* - output port for eQEP position-compare synchronous output pulse stretcher
- *QFLG.INT* - output port for eQEP interrupt flag

Encoder

An encoder is connected to the machine rotor and generates two quadrature signals as well as a quadrature index signal. An example of an optical encoder



Optical encoder disk with QEPI signal gated to QEPB [1]

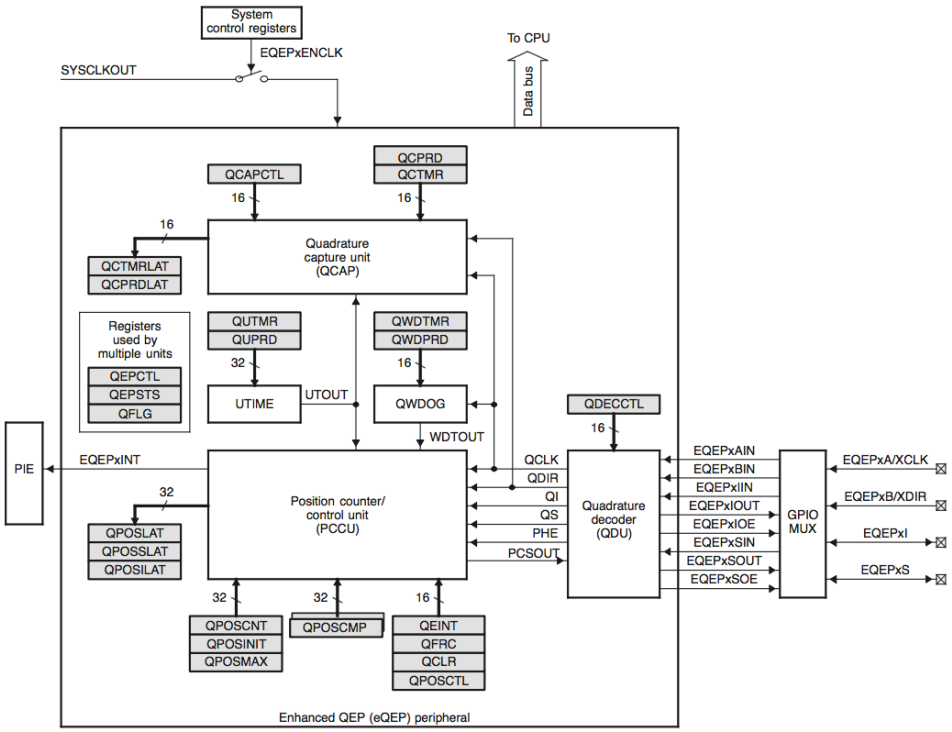
is shown above. The number of slots of the encoder is the track of dark/light line pairs that occur per revolution. These slots create an alternating pattern of dark and light lines. The lines on the disk are read by two different photo-elements that are mechanically shifted by a quarter of the pitch of the line pair between them. As the disk rotates, the two photo-elements generate signals that are shifted 90-degrees out of phase from each other. These are usually referred to as the QEPA and QEPB signals. Additionally, a second track is added to generate a signal that occurs once per revolution. This signal can be used to indicate an absolute position and is known as the QEPI signal. Different manufacturers often refer to this signal as index, marker, home position, and zero reference [1].

The QEPA, QEPB, and QEPI signals are read as inputs by the Quadrature Decoder Unit (QDU).

eQEP Module Overview

The figure below shows the major functional overview of the eQEP peripheral. The PLECS Type 0 eQEP module provides the following functional units:

- Quadrature Decoder Unit
- Position Counter and Control Unit
- Edge Capture Unit
- Interrupt Generation



Functional Block Diagram of the eQEP Peripheral [1]

Quadrature Decoder Unit

The Type 0 eQEP Quadrature Decoder Unite (QDU) can be configured to operate in Quadrature-count, Direction-count, UP-count, and DOWN-count

modes. However, the PLECS eQEP Type 0 module only supports operation in Quadrature-count mode.

Note Direction-count, UP-count, and DOWN-count modes are not supported in the PLECS eQEP Type 0 module.

Quadrature-count mode, the QEPA and QEPB signals are used to determine the direction of rotation and the information is updated in the *QDF* bit in the *QEPSTS* register. This bit is provided as an output of the PLECS eQEP module. The QEPA and QEPB signals are sensed to determine when the position counter is to be incremented/decremented. At each edge of the QEPA/B signal, an eQEP clock pulse is generated (QCLK). The QCLK and QDF bits determine if the counter should be incremented or decremented.

The QDU can be configured to operate such that QEPA and QEPB signals are fed to the QA and QB inputs, respectively, for normal operation. The QDU can also be configured such that QEPA and QEPB signals are fed to the QB and QA inputs, respectively, to reverse the count direction. The *SWAP* bit in the *QDECCTL* register is used to control this.

The QCLK generated by the eQEP occurs at a rate that is four times the frequency of the input signals. The generation of the high frequency QCLK signal can be avoided by lumping the encoder and QDU models. A simplified model of the encoder and QDU is incorporated into the PLECS eQEP model. The encoder, attached to the mechanical input of the PLECS eQEP model, converts the rotation of the mechanical port into the equivalent effect on the eQEP counter. It does not generate the QEPA or QEPB signals internally and thus has some inherent limitations.

Note A 2000-line encoder directly coupled to a motor running at 5000 revolution per minute would result in a QEPA or QEPB frequency of 166.6 KHz (or 6 μs) [1].The phase shift between the QEPA and QEPB signals would require the solver to take steps every 1.5 μs. This would cause the simulation speed to be extremely slow. To mitigate this issue the encoder and QDU are lumped together in a simplified model.

It is assumed that the encoder does not have any non-idealities and the QEPA and QEPB signals are perfectly phase-shifted by 90 degrees. Thus a Phase Er-

ror Flag will never be generated for the PLECS eQEP model and is not modeled.

Position Counter and Control Unit

The PLECS eQEP module can be operate in the following modes:

- Position Counter Reset on Index Event
- Position Counter Reset on Maximum Position
- Position Counter Reset on the First Index Event

In all of these modes, the position counter is reset to 0 on overflow and to QPOSMAX on underflow. Overflow occurs when the counter tries to counts up past QPOSMAX and underflow occurs when the counter tries to counts down past 0. Interrupt flags can be set on an overflow or underflow event.

Note The PLECS eQEP module does not support position counter reset on unit time out event mode.

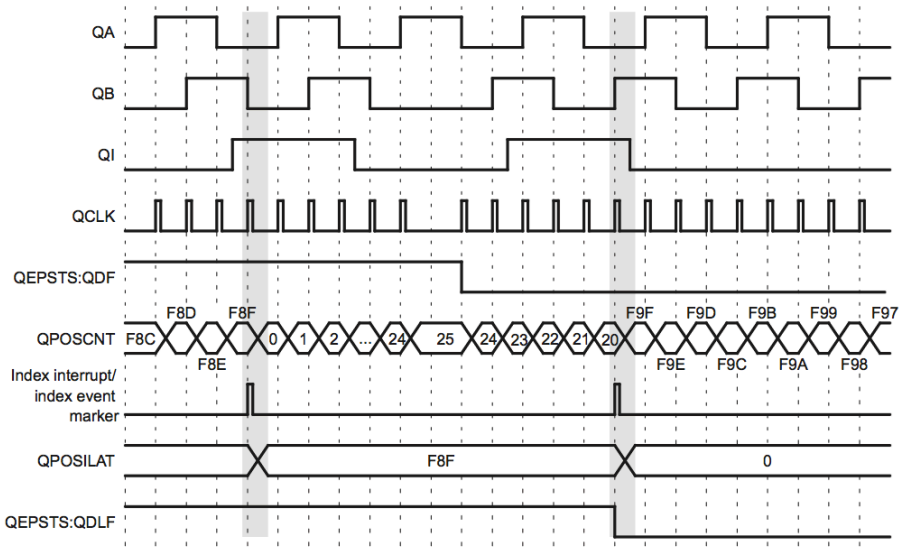
Position Counter Reset on Index Event

In the position counter reset on index event (PCROI) mode, the position counter is reset to 0 if an index event occurs during forward motion, and to QPOSMAX in the reverse motion. In the PLECS eQEP module, the QEPA and QEPB signals are not generated internally and thus eQEP clock resolution is limited. It is assumed that the index event coincides with the edges of the QEPI signal. Further, the QPOSMAX value must be chosen such that the maximum number of counts in one complete revolution is an integer multiple of (QPOSMAX + 1).

When used with high pole-pair machines, the counter can overflow/underflow multiple times in between index events. This allows the PLECS eQEP module to be configured to capture the "electrical" position of the rotor.

Note In PCROI mode, the QPOSMAX value must be chosen such that the maximum number of increments in one complete revolution is an integer multiple of (QPOSMAX + 1).

The figure below shows the operation of a 1000-line encoder with QPOSMAX set to 3999 and operated in PCROI mode.

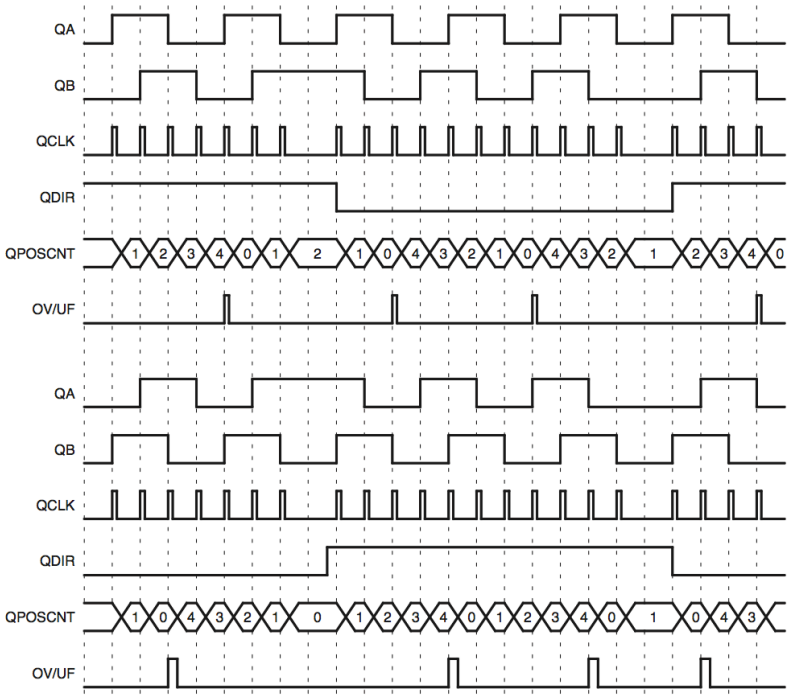


Position counter reset by index pulse for 1000 Line encoder (QPOSMAX = 3999) [1]

Position Counter Reset on Max Position

In Position Counter Reset on Max Position (PCROMP) mode, the position counter counts up to QPOSMAX in forward motion and is reset to 0 on the next eQEP clock event. In the reverse motion, the counter counts down to 0 and is reset to QPOSMAX on the next eQEP clock event. The corresponding overflow and underflow flags are generated at these events.

The figure below shows the operation of the eQEP in PCROMP mode with QPOSMAX set to 4.



Position counter underflow/overflow (QPOSMAX = 4) [1]

Note In the PLECS eQEP module, the initial counter value (QPOSINIT) must be set between 0 and QPOSMAX, in PCROMP mode.

Position Counter Reset on First Index Event

In the Position Counter Reset on the First Index Event (PCTFIE) mode, the counter is reset to 0 if an index event occurs in forward motion and QPOSMAX if it occurs in reverse motion. This only occurs on the first occurrence and subsequently the position counter is reset based on maximum position. For a detailed description of the operation of the PCROMP, see the section above.

Note In the PLECS eQEP module, in both PCTFIE and PCROI modes, the counter is reset at the immediate occurrence of a QEPI signal due to limited resolution of the QCLK. This is because the QEPA and QEPB signals are not generated internally.

Position Compare Unit

The eQEP can be used to generate a sync output and/or interrupt on a position compare match event. The position compare (*QPOSCMP*) is operated in shadow-mode only in the PLECS eQEP module. The shadow register value is transferred into the active register on the following events: load on compare match or load on position counter zero event.

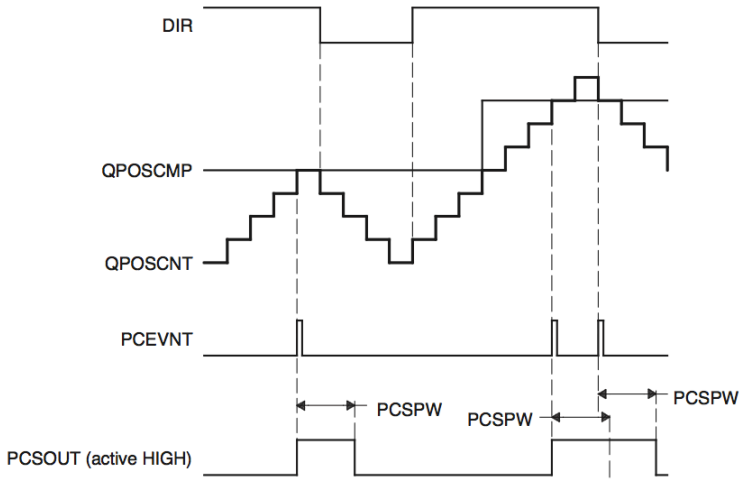
A programmable position compare sync output signal is generated on a position compare match event. In the event of a new position compare match while a previous position compare pulse is still active, the pulse stretcher generates a pulse of a specified duration from the new position compare event, as shown in the figure below.

Note Shadow mode can not be disabled for the PLECS eQEP position compare unit.

Edge Capture Unit

The eQEP module consists of an inbuilt edge capture unit that can capture position and time information to determine the rotor speed. This enables the calculation of rotor speed by the following equations:

$$v(k) \approx \frac{x(k) - x(k-1)}{T} \tag{3.1}$$



eQEP position compare Sync output pulse stretcher [1]

$$v(k) \approx \frac{X}{t(k) - t(k-1)} \tag{3.2}$$

Equation 3.1 is typically used to measure speed when the rotor is at high speed. In this method a unit timer is configured to read the position counter once every interval. The unit timer can be enabled or disabled by configuring the *UTE* bit in the *QEPCTL* register. The timer counter (*QUTMR*) is timed at the system clock frequency and counts up. When it counts up to the period register (*QUPRD*) the counter is reset to zero and the *QFLG.UTO* bit is set. The reset event also causes the position counter value to be latched into the *QPOSLAT* register. Thus to determine the speed, equation 3.1 can be used as follows:

$$v(k) \approx \frac{QPOSLAT(k) - QPOSLAT(k-1)}{QUPRD + 1} \times \frac{2 \times \pi \times SYSCLKOUT}{4 \times NumberOfSlots} \tag{3.3}$$

In equation 3.3, *QPOSLAT(k) - QPOSLAT(k-1)* gives the number of counts be-

tween two unit time out event. At each *QCLK* event, the rotor displacement of $\frac{2\pi}{4\times NumberOfSlots}$ occurs in *radians*. Thus the total displacement of the rotor can be determine by scaling the number of counts between two unit time out events by the displacement in *radians* per count. The time interval can be determined as $\frac{SYSCLKOUT}{QUPRD+1}$, where *SYSCLKOUT* is the System Clock frequency in Hz.

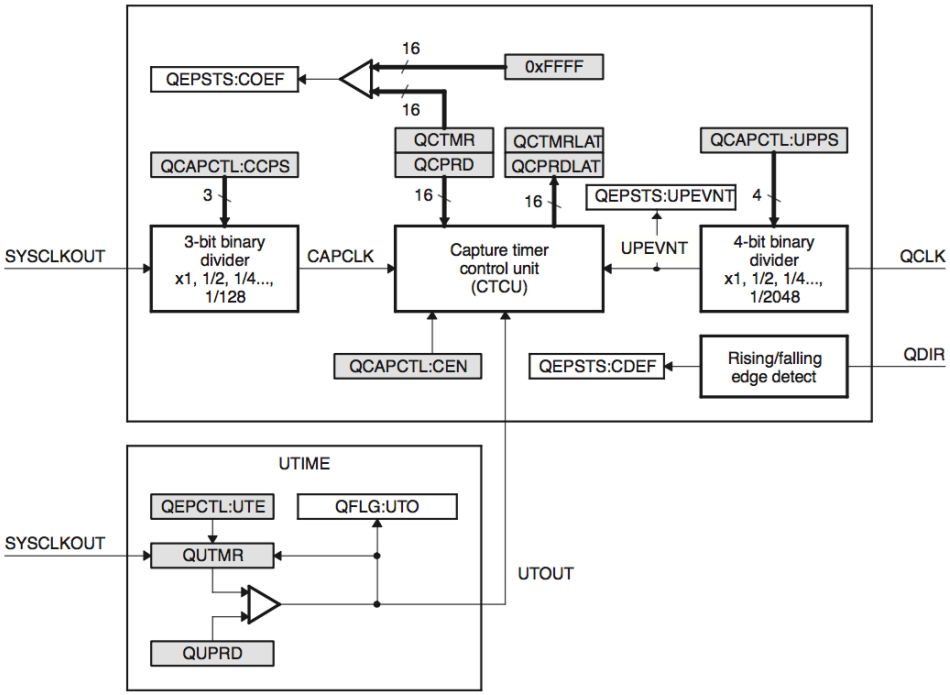
At low speeds, the configuration of the system may result in inaccurate estimation of the speed. In a 500-line per revolution encoder with velocity calculation at a rate of 400 Hz the minimum detectable speed is 12 rpm. Below this the edge capture unit can not accurately estimate the velocity [1].

The edge capture unit also has a timer (*CAPCLK*) that runs at a prescaled rate of the *SYSCLKOUT*. This inner counter is clocked at *CAPCLK* and counts the number of clock periods that occur between a predetermined number of *QCLK* counts. This allows the resolution to be increased at the slow speeds. capture timer (*QCTMR*) is latched into the capture period register (*QCPRD*) on every unit position event and the timer is reset. A flag is set in the *QEPSTS* register to indicate that a new value has been latched into the QCPRD register [1]. In a similar fashion the speed can be estimates as:

$$v(k) \approx \frac{2^{QCAPCTL.UPPS}}{QCPRD+1} \times \frac{2\times\pi\times CAPCLK}{4\times NumberOfSlots} \tag{3.4}$$

In equation 3.4, QCPRD gives the counter timer value when an unit position event occurs. The total distance travelled between the unit position is given by $2^{QCAPCTL.UPPS} \times \frac{2\pi}{4\times NumberOfSlots}$ in *radians*. The total time taken during the unit position events is determined as $\frac{CAPCLK}{QCPRD+1}$, where *CAPCLK* is the capture unit clock frequency in Hz.

In both cases, the calculations are only accurate if the direction doesn't change in-between two consecutive measurements. In the event of a direction change occurring between two unit position event, a change of direction error flag (*QEPSTS.CDEF*) is set. Further, the measurements are also inaccurate if the timer counts more than 65535 counts between two unit position events. In this event an overflow flag (*QEPSTS.COEF*) is set.



eQEP edge capture unit [1]

Note Measurements done for low speed calculation can lead to the creation of a high frequency signal when the rotor speed is high. Users specify a low speed threshold beyond which the measurements done for low speed calculation are disabled. This ensures simulation efficiency when the rotor speed is high.

---

eQEP Interrupt

The PLECS eQEP module can be configured to generate interrupts by configuring the following bits in the *QEINT* register:

- *QDC* - enables interrupt generation due to direction change.

- *PCU* - enables interrupt generation due to position counter underflow.
- *PCO* - enables interrupt generation due to position counter overflow.
- *PCM* - enables interrupt generation due to position compare match event.
- *UTO* - enables interrupt generation due to unit time out event.

Note Flags used to generate the interrupt signal are automatically cleared in the PLECS eQEP module after one system clock period for ease of use.

Summary of PLECS Implementation

The PLECS eQEP module models the major functionality of the actual TI type 0 eQEP module. Below is a summary of the differences between the PLECS Type 0 eQEP module and the actual Type 0 eQEP module:

- Direction-count, UP-count, and DOWN-count modes are not supported in the PLECS eQEP Type 0 module.
- The PLECS eQEP module does not support position counter reset on unit time out event mode.
- In PCROI mode, the QPOSMAX value must be chosen such that the maximum number of increments in one complete revolution is an integer multiple of (QPOSMAX + 1). (see page 116)
- In the PLECS eQEP module, the initial counter value (QPOSINIT) must be set between 0 and QPOSMAX, in PCROMP mode. (see page 117)
- In the PLECS eQEP module, in both PCTFIE and PCROI modes, the counter is reset at the immediate occurrence of a QEPI signal due to limited resolution of the QCLK. This is a result of the fact that QEPA and QEPB signals are not generated internally. (see page 118)
- Shadow mode can not be disabled for the eQEP position compare unit.
- Measurements done for low speed calculation can lead to the creation of a high frequency signal when the rotor speed is high. Users specify a low speed threshold beyond which the measurements done for low speed calculation are disabled. This ensures simulation efficiency when the rotor speed is high.
- Flags used to generate the interrupt signal are automatically cleared.

Reference

1 - Pictures provided with Courtesy of Texas Instruments, Literature source: *TMS320x2806x Piccolo Technical Reference Manual*, Literature Number SPRUH18D, January 2011-February 2013

2 - Pictures provided with Courtesy of Texas Instruments, Literature source: *TMS320x2833x Analog-to-Digital Converter (ADC) Module Reference Guide*, Literature Number SPRU812A, September 2007 - Revised October 2007

3 - Pictures provided with Courtesy of Texas Instruments, Literature source: *TMS320x2833x, 2823x Enhanced Capture (eCAP) Module Reference Guide*, Literature Number: SPRUFG4A, August 2008 - Revised June 2009

4 - Pictures provided with Courtesy of Texas Instruments, Literature source: *TMS320x2837xD, 2827xD Analog-to-Digital Converter (ADC) Module Reference Guide*, Literature Number: SPRUHM8C, December 2013 - Revised December 2014

4

STM32 F0xx Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

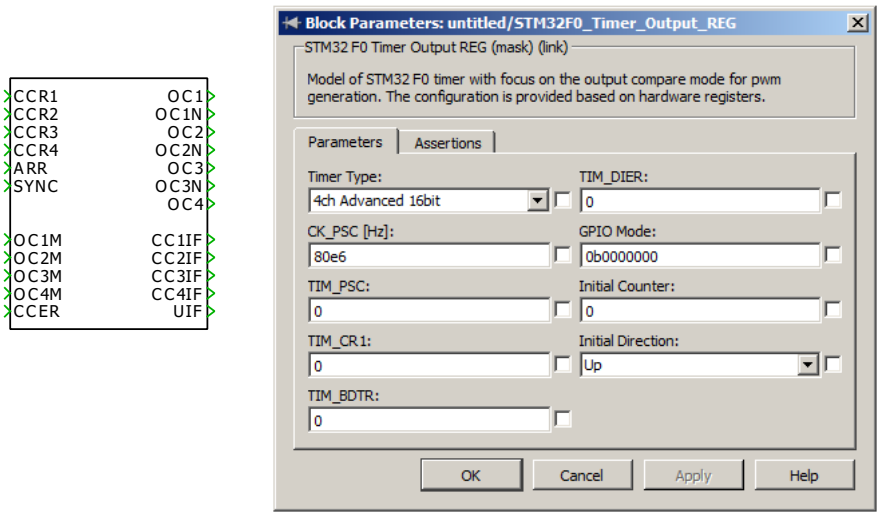
The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

System Timer for PWM Generation (Output Mode)

The PLECS peripheral library provides two blocks for the STM32 F0 system timer used in output mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer model for output mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Timer Subtypes

The STM32 F0 MCU's provide several subtypes of timers which can be used for input capture, output compare and PWM generation functionalities. In the presented model, all subtypes listed below are combined in one module and can be chosen via the component mask:

- 4 Channel 16bit Advanced Timer
- 4 Channel 16bit General Purpose Timer
- 4 Channel 32bit General Purpose Timer
- 2 Channel 16bit GP Timer with Complementary Outputs and Deadtime
- 1 Channel 16bit GP Timer with Complementary Outputs and Deadtime
- 1 Channel 16bit General Purpose Timer

The focus of this model is the timer output behavior meaning that all input functionalities are disregarded. This corresponds to the hardware behavior with all TIM_CCMRx.CCyS cells being set to 00. Further, the One-Shot mode of the module is not supported. In the following sections, the common part of all subtypes is explained together with the models limitations. Further, the differences between the subtypes are described in more detail.

General Counter Behavior

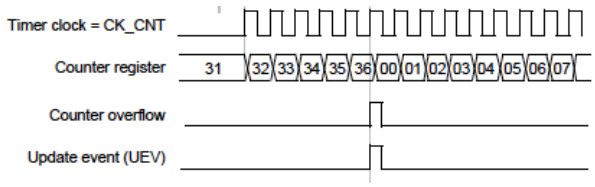
The base of all timer modules is an auto-reload counter driven by a prescaled counter clock *CK_CNT*. The period of this time base clock is determined by the counter clock frequency *CK_PSC* and the prescaler register *TIM_PSC*, both configurable in the mask, as follows:

$$T_{CK\_CNT} = \frac{TIM\_PSC + 1}{CK\_PSC}$$

The counter either operates in Edge-aligned mode with configurable direction or in Center-aligned mode. In addition to the general counter functionality, the module also generates output compare interrupt flags when the counter matches the values stored in the *CCRx* registers. Those flags are later used to determine the output levels of the timer module.

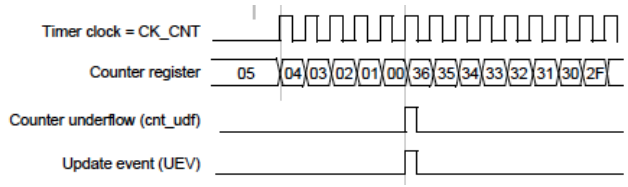
Edge-aligned mode

In upcounting direction, the counter counts from 0 to the counter period value *TIM_ARR* and generates an update event *UEV* simultaneous to the counter overflow.



Edge-aligned mode / Upcounting [1]

In downcounting direction, the counter counts from *TIM_ARR* to 0 and generates an update event (*UEV*) simultaneous to the counter underflow.



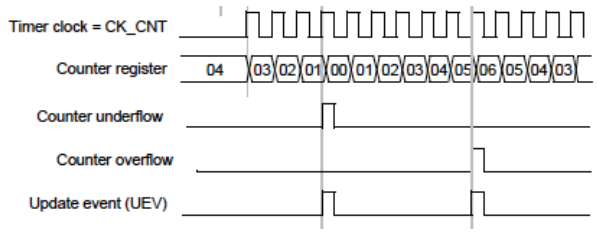
Edge-aligned mode / Downcounting [1]

In Edge-aligned mode, the counter period and therefore the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot (TIM\_ARR + 1)$$

Center-aligned mode

In this mode, the counter alternates its direction and generates an update event (*UEV*) at the counter under- and overflow.

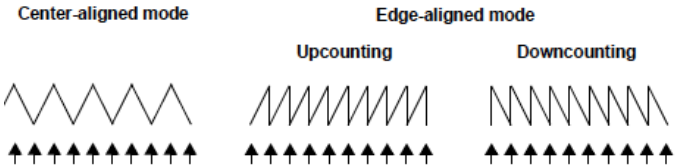


Center-aligned mode [1]

For Center-aligned mode, the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot 2 \cdot TIM\_ARR$$

For all modes, the timer model operates in preloaded mode, meaning that the used configuration is updated simultaneously to the update events. The Repetition Counter functionality is not supported in the model.



Events used for configuration update [1]

In other words, all input terminals of the model, except the *CCER* register, are sampled with the instants of the update events.

The timer mode, direction and output compare flag behavior can be set jointly using the *TIM_CR1* register.

Timer Mode Configuration

The *CKD* field only has an effect on the subtypes with PWM dead time generation and is therefore described in a later section. The register cell *CMS* can be used to determine the counter mode and the output compare flag behavior.

- 00 - Edge-aligned mode
- 01 - Center-aligned mode 1 - compare flags only set when counting down
- 10 - Center-aligned mode 2 - compare flags only set when counting up
- 11 - Center-aligned mode 3 - compare flags set when counting up and down

In Edge-aligned mode, the *DIR* bit determines the counter direction.

- 0 - Upcounting
- 1 - Downcounting

The module assumes the timer as always active and to be operated in preloaded mode with the update event generation always enabled. Therefore, the following settings are mandatory when using the register-based version.

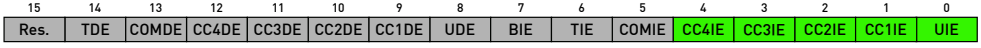
- TIM_CR1.ARPE = 1
- TIM_CR1.UDIS = 0
- TIM_CR1.CEN = 1

Initialization and Synchronization

The timer allows a counter initialization in the component mask. Further, the initial counter direction can be specified which only affects the Center-Aligned Mode. With a positive flank at the SYNC terminal, the counter is reset to zero and the dynamic configuration is updated. The initialization and synchronization features enable time-shifted pwm signals using multiple timer modules.

Interrupt Flags

The timer module can generate interrupt flags at the *CCxIF* and *UIF* output terminals. Those flags are based on the counter compare and update event flags and can be used in the model to, i.e., trigger an ADC conversion or a new control step via the PIL block. Note that in the model those flags are implemented as pulses.



Interrupt enable register

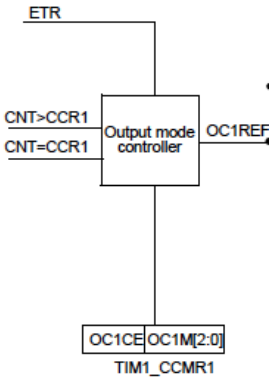
The interrupt flags can be enabled with the bits of the *TIM_DIER* register.

- 0 - interrupt disabled
- 1 - interrupt enabled

Note Only the four channel subtype implementations make use of all *CCxIE* fields.

Output Mode Controller

The output-mode controller generates up to 4 reference signals *OCyREF* based on the output compare flags of the counter.



Output Mode Controller for *OCyREF* [1]

The controller implements several output modes defining the behavior of *OCyREF*. With the register fields *TIM_CCMRx.OCyM*, the mode of each reference signal can be specified separately.

- 000 - Frozen, comparisons have no effect on *OCyREF*
- 001 - Active match mode, *OCyREF* forced high when $CTR = CCRy$
- 010 - Inactive match mode, *OCyREF* forced low when $CTR = CCRy$
- 011 - Toggle mode, *OCyREF* toggled when $CTR = CCRy$
- 100 - Force inactive mode, *OCyREF* always forced low
- 101 - Force active mode, *OCyREF* always forced high
- 110 - PWM Mode 1
- 111 - PWM Mode 2

Because the reference signal mode is supposed to be changed during simulation, the OCyM fields can be accessed via the input terminals. Note that those are also updated with the update events generated by the timer.

The hardware options to externally clear the reference signal are not supported in the model. Further, the break function of the timer is not part of the model assuming the flag *BDTR.MOE* is always set. Therefore it is mandatory to set *MOE* to 1 while using the resister-based version.

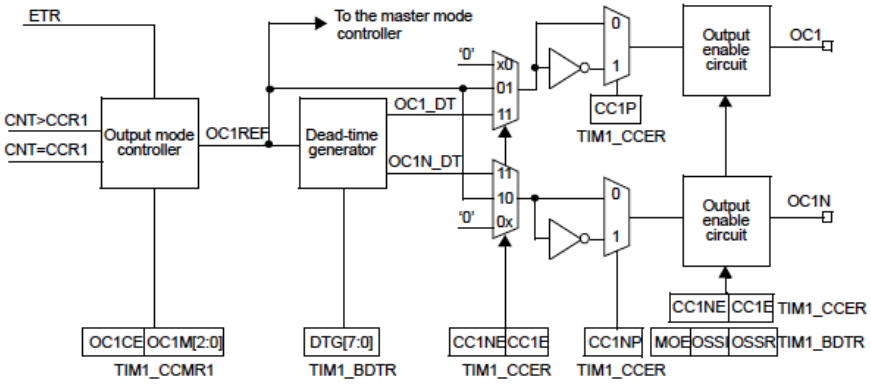
The options available in the output stage majorly depend on the timer subtype and therefore are discussed in the subsequent sections. The configuration of all output stages is done with the *CCER* register.

Note The *CCER* is accessed via the input terminals and is not preloaded. This means that a change on the *CCER* input directly effects the outputs.

---

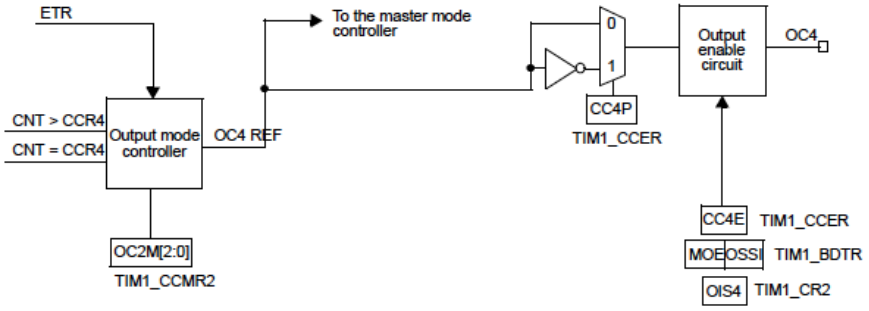
4 Channel Advanced Timer

The Advanced Timer consists of a timer and a 4 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned (up and down) as well as Center-aligned mode. For channels 1 to 3, the output stage enables complementary outputs with dead time and configurable polarity.



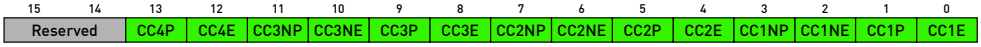
Output stage of Advanced Timer (channel 1 to 3) [1]

For channel 4, the output stage shown below only supports configurable polarity.



Output stage of Advanced Timer (channel 4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channels 1 to 3. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$

- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

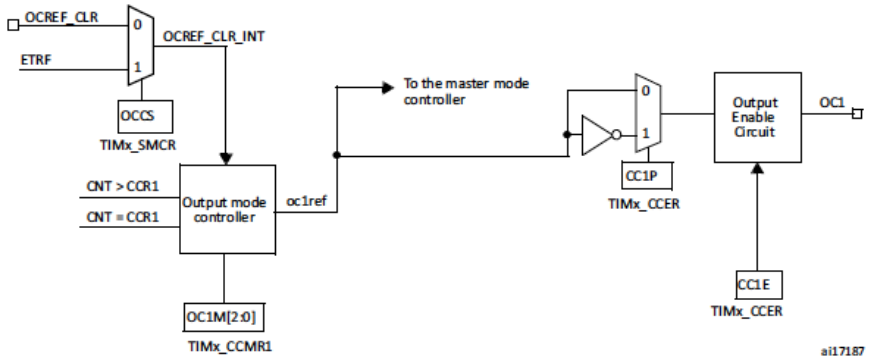
The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

This subtype implementation uses the full set of inputs, outputs and configuration registers.

4 Channel General Purpose Timer

This subtype is available with a 16-bit or 32-bit counter implementation both supporting Edge-aligned (up and down), as well as Center-aligned modes. The 4 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4NP	Res.	CC4P	CC4E	CC3NP	Res.	CC3P	CC3E	CC2NP	Res.	CC2P	CC2E	CC1NP	Res.	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

The terminals used by this subtype are shown in the table below.

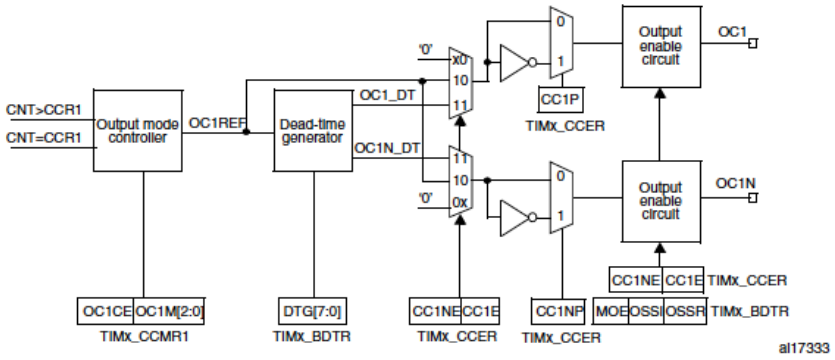
Terminal Group	Utilized	Unused
Input	CCR1 - CCR4, ARR, SYNC, OC1M - OC4M, CCER	x
Output	OC1 - OC4, CC1IF-CC4IF, UIF	OC1N - OC3N

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- GPIO Mode for unused outputs

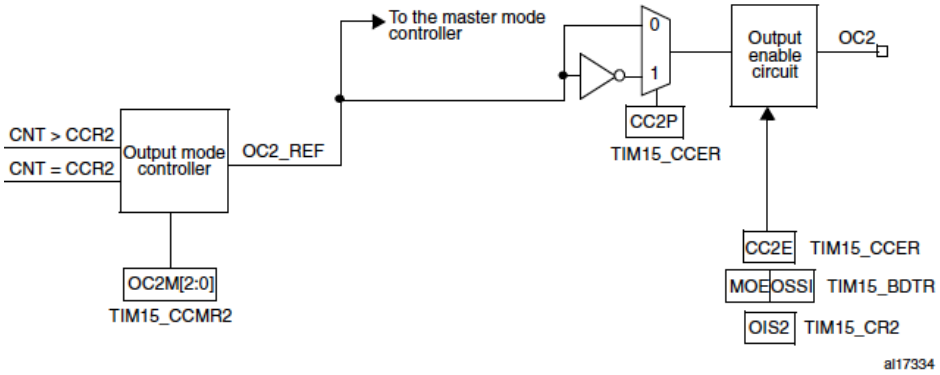
2 Channel Complementary GP Timer with Deadtime

This subtype consists of a timer and a 2 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned in upward direction. For channel 1 the output stage enables complementary outputs with dead time and configurable polarity.



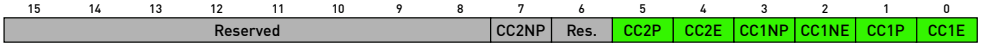
Output stage of Complementary GP Timer (channel 1) [1]

For channel 2, the output stage shown below only supports configurable polarity.



Output stage of Complementary GP Timer (channel 2) [1]

The *CCER* register can be used to configure the channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channel 1. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$

- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

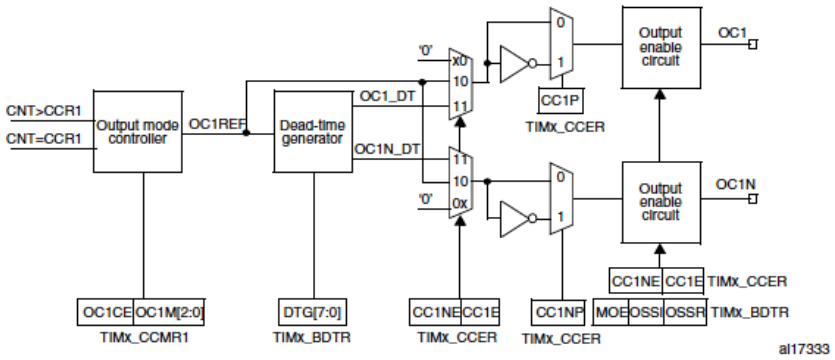
Terminal Group	Utilized	Unused
Input	CCR1 - CCR2, ARR, SYNC, OC1M - OC2M, CCER	CCR3 - CCR4, OC3M-OC4M
Output	OC1 - OC2, OC1N, CC1IF - CC2IF, UIF	OC3 - OC4, OC2N - OC3N, CC3IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC3IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel Complementary GP Timer with Deadtime

This subtype consists of a timer and a single channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned in upward direction. The output stage enables complementary outputs with dead time and configurable polarity on channel 1.



Output stage of Complementary GP Timer (channel 1) [1]

The *CCER* register can be used to configure the channels of the output stage separately.

Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channel 1. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

Dead time configuration

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

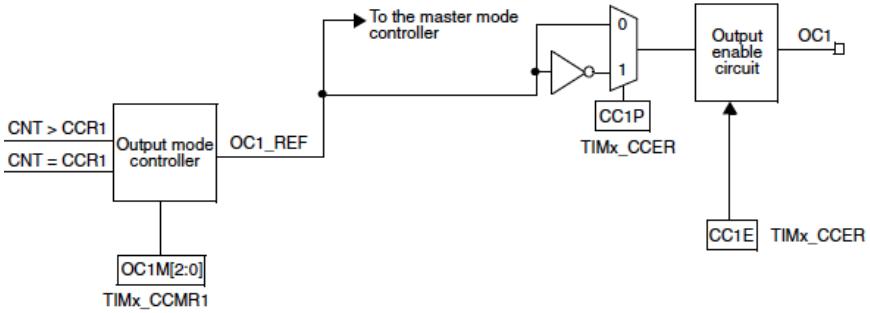
Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR4, OC2M-OC4M
Output	OC1, OC1N, CC1IF, UIF	OC2 - OC4, OC2N - OC3N, CC2IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The single channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/1) [1]

The *CCER* register can be used to configure the single channel output stage.

Configuration of the output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CC1NP bit has no effect on the model.

The terminals used by this subtype are shown in the table below.

Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR4, OC2M-OC4M
Output	OC1, CC1IF, UIF	OC2 - OC4, OC1N - OC3N, CC2IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

GPIO Mode

In case that an output enable circuit is configured as inactive, the output level is determined by the GPIO Mode. To mimic this in the simulation model, the parameter GPIO Mode is available in the register-based version.

Configuration of GPIO Mode

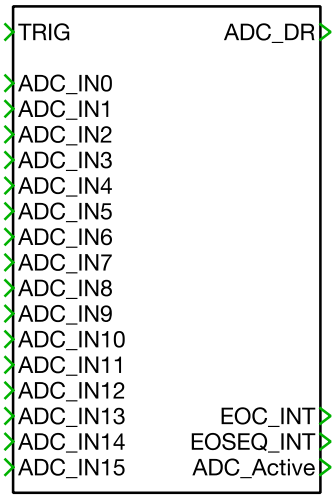
With the bits *OCx* and *OCxN*, the corresponding output mode can be set.

- 0 - Pull-Down (Inactive Low)
- 1 - Pull-Up (Inactive High)

Note This Register is available only in the simulation.

Analog-Digital Converter (ADC)

The PLECS peripheral library provides two blocks for the STM32 F0 ADC module, one with a register-based configuration mask and a second with a GUI. The figure below shows the appearance of the block.



ADC module model

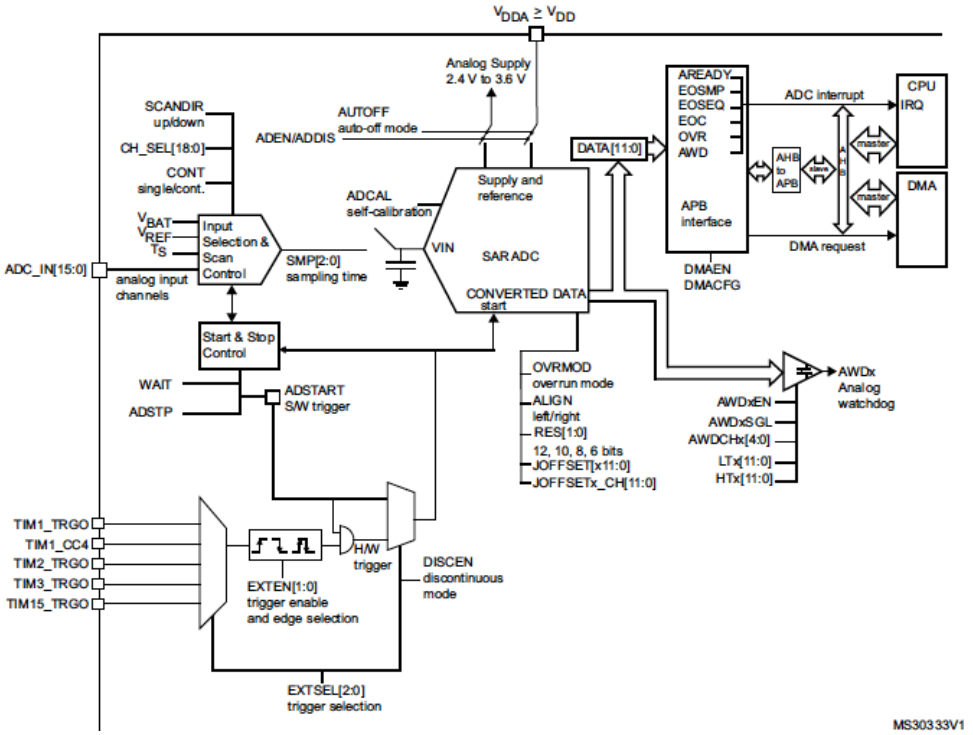
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *TRIG* - input port to trigger adc conversions
- *ADC_INx* - input measurement channels
- *ADC_DR* - output port to access conversion results
- *EOC_INT* - output port for subsequent logic triggered by a conversion end
- *EOSEQ_INT* - output port for subsequent logic triggered by a sequence end
- *ADC_Active* - output port indicating an active conversion

ADC Module Overview

The PLECS ADC model contains the most relevant features of the MCU peripheral.



Overview of the STM F0 ADC module [1]

The ADC model implements these logical submodules:

- ADC Converter with Result Registers
- ADC Sample Logic for Single and Discontinuous mode
- ADC Interrupt Logic

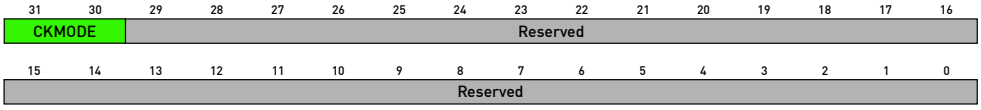
For simplicity, the external trigger configuration shown in the figure above is neglected. The trigger to the converter is directly accessed via the *TRIG* terminal. Further, the Analog Watchdog, DMA and ADC overrun functionalities as well as the related interrupts are not part of the model. Due to simulation efficiency reasons, the adc can not be operated in continuous conversion mode.

While the adc is active, incoming triggers are lost. Stopping a conversion is not supported within the model.

ADC Converter with Result Registers

The ADC module contains a converter with configurable resolution. An external voltage reference is used which can be defined in the component mask.

The period of the ADC clock, and therefore the time base of the module, can be determined based on *PCLK* with a prescaler or can be set to an asynchronous clock of 14 MHz.



ADC_CFGR2 Register structure

By using the field *ADC_CFRG2.CKMODE* the ADC time base can be specified as follows:

CKMODE	ADC clock
00	14 MHz
01	PCLK / 2
10	PCLK / 4
11	not supported

The resolution of the converter can be specified with the fields *RES* of the *ADC_CFGR1* register given in the next section. This also influences the amount of ADC clock cycles needed for a conversion. With the *RES* bits the resolution can be specified as shown in the table below.

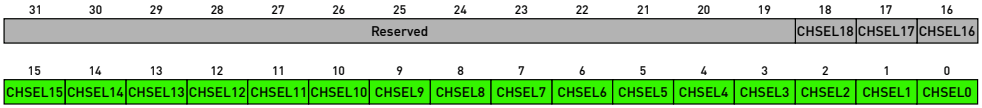
RES[1]	RES[0]	Resolution	Conversion length
0	0	12 bit	12.5 ADCCLK cycles
0	1	10 bit	11.5 ADCCLK cycles
1	0	8 bit	9.5 ADCCLK cycles
1	1	6 bit	7.5 ADCCLK cycles

For the conversion results, the hardware adc contains a single 16-bit result register *ADC_DR*. The results of multiple, sequential conversions are typically moved to the *SRAM* on the fly via the *DMA controller*. To simplify this, the *ADC_DR* terminal provides the conversion result for each of the 16 possible sequence members separately. For example, the second signal of the *ADC_DR* terminal holds the conversion results of *ADC_IN1*.

The component further only supports the right aligned result representation mode meaning that *ADC_CFGR2.ALIGN* always needs to be set to 0. In addition to this, the model provides an option to represent the conversion results as quantized double integers, which can be chosen with the mask parameter **Output Mode**.

ADC Sample Logic

The STM32F0 ADC is a sequencer type adc converting the channels specified within a conversion sequence. The register *ADC_CHSELR* defines the channels part of the sequence.

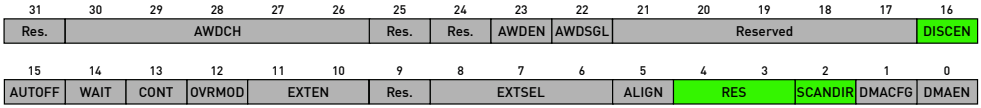


ADC_CHSELR Register structure

Note that *CH16-CH18* cannot be chosen because the measurements for the temperature sensor as well as the internal reference and the battery voltage are not part of the model.

The adc model implements the single and discontinuous conversion modes of the adc. The continuous conversion mode is not supported due to simulation efficiency reasons.

The *ADC_CFGR1* register is applied to choose the ADC conversion mode and control the direction.



ADC_CFGR1 Register structure

In single conversion mode (*DISCEN = 0*), the adc, once triggered, performs a full sequence of conversions for all channels defined in the *ADC_CHSELR* register.

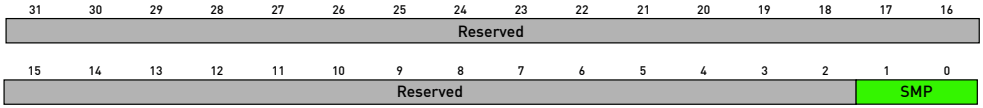
In discontinuous conversion mode (*DISCEN = 1*), the adc, once triggered, only converts a single channel of the sequence.

With the bit *SCANDIR*, the user can specify if the sequence starts with the lowest channel or the highest channel specified.

Note The adc model assumes the adc not to operate in continuous conversion mode and to be always active. Therefore *ADC_CFGR1.CONT* needs to be cleared while using the register-based configuration.

SCANDIR	Scan direction
0	ADC_IN0 to ADC_IN15
1	ADC_IN15 to ADC_IN0

The sample time of the adc is configurable and can be set using the *ADC_SMPR* register.

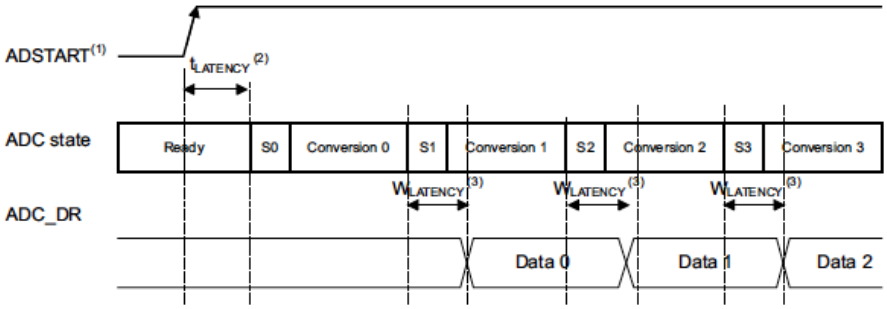


ADC_SMPR Register structure

SMP	Sampling Time
000	1.5 cycles
001	7.5 cycles
010	13.5 cycles
011	28.5 cycles
100	41.5 cycles
101	55.5 cycles
110	71.5 cycles
111	239.5 cycles

ADC Trigger and Register Write Latency

According to the STM32F0 ADC manual, the hardware module has some trigger and register write latency as indicated in the picture below.

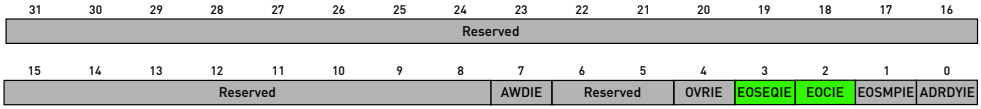


ADC trigger and register write latency

The trigger latency can be chosen to multiples of the ADC clock via a combo box in the component mask. Due to the fact that a trigger is synched to a positive edge of the ADC clock, the delay between a trigger and the sampling start can be the latency specified plus up to one ADC clock period. The register write latency is entered directly and should not exceed the length of a full sampling and conversion process.

ADC Interrupt Logic

The ADC module also has a connection to the *NVIC* of the *STM F0 MCU*. The *EOC* flag is set after each single conversion and the *EOSEQ* flag at the end of the sequence. The register *ADC_IER* can be used to configure the adc to provide an interrupt pulse to the corresponding output terminals.



ADC_IER Register structure

- 0 - no interrupt pulses generated at the EOC_INT/EOSEQ_INT terminal
- 1 - interrupt pulses generated at the EOC_INT/EOSEQ_INT terminal

Even if there typically won't be a model of the *NVIC* within the simulation, those pulses can i.e. be used to trigger the PIL block modeling a control step triggered by a finished adc conversion.

Reference

1 - Literature Source: STM32 Reference Manual [RM0091]

5

STM32 F1xx Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

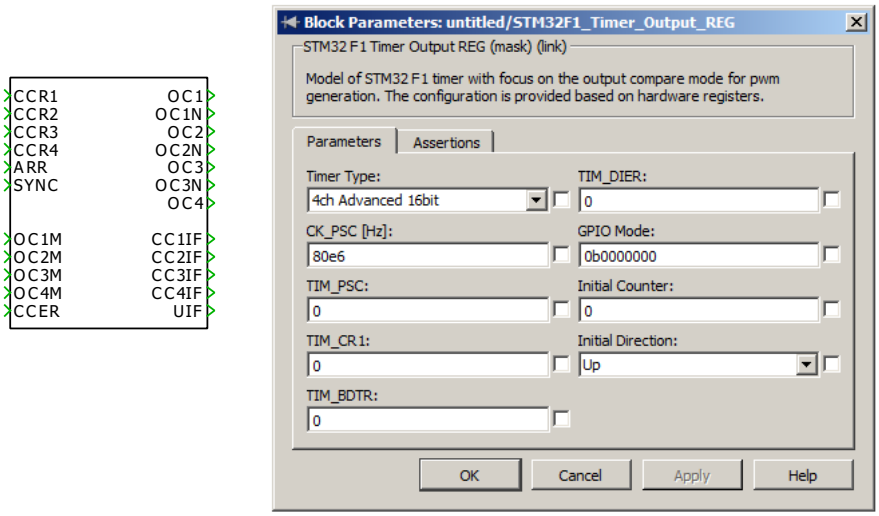
The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

System Timer for PWM Generation (Output Mode)

The PLECS peripheral library provides two blocks for the STM32 F1 system timer used in output mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer model for output mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Timer Subtypes

The STM32 F1 MCU's provide several subtypes of timers which can be used for input capture, output compare and PWM generation functionalities. In the presented model, all subtypes listed below are combined in one module and can be chosen via the component mask:

- 4 Channel 16bit Advanced Timer
- 4 Channel 16bit General Purpose Timer
- 2 Channel 16bit GP Timer with Complementary Outputs and Deadtime
- 1 Channel 16bit GP Timer with Complementary Outputs and Deadtime
- 2 Channel 16bit General Purpose Timer
- 1 Channel 16bit General Purpose Timer

The focus of this model is the timer output behavior meaning that all input functionalities are disregarded. This corresponds to the hardware behavior with all TIM_CCMRx.CCyS cells being set to 00. Further, the One-Shot mode of the module is not supported. In the following sections, the common part of all subtypes is explained together with the models limitations. Further, the differences between the subtypes are described in more detail.

General Counter Behavior

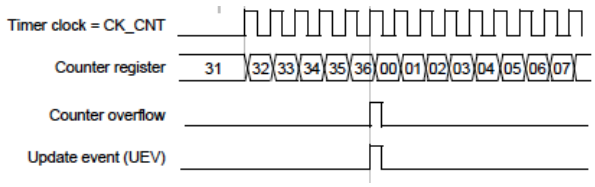
The base of all timer modules is an auto-reload counter driven by a prescaled counter clock *CK_CNT*. The period of this time base clock is determined by the counter clock frequency *CK_PSC* and the prescaler register *TIM_PSC*, both configurable in the mask, as follows:

$$T_{CK\_CNT} = \frac{TIM\_PSC + 1}{CK\_PSC}$$

The counter either operates in Edge-aligned mode with configurable direction or in Center-aligned mode. In addition to the general counter functionality, the module also generates output compare interrupt flags when the counter matches the values stored in the *CCRx* registers. Those flags are later used to determine the output levels of the timer module.

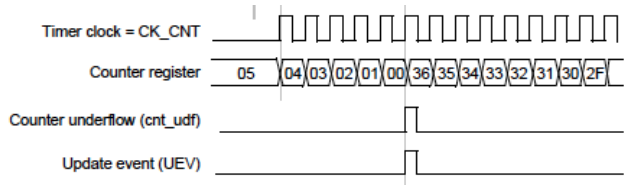
Edge-aligned mode

In upcounting direction, the counter counts from 0 to the counter period value *TIM_ARR* and generates an update event *UEV* simultaneous to the counter overflow.



Edge-aligned mode / Upcounting [1]

In downcounting direction, the counter counts from *TIM_ARR* to 0 and generates an update event (*UEV*) simultaneous to the counter underflow.



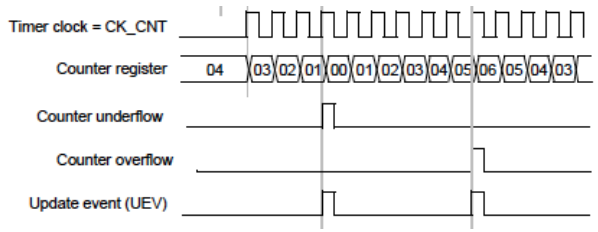
Edge-aligned mode / Downcounting [1]

In Edge-aligned mode, the counter period and therefore the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot (TIM\_ARR + 1)$$

Center-aligned mode

In this mode, the counter alternates its direction and generates an update event (*UEV*) at the counter under- and overflow.

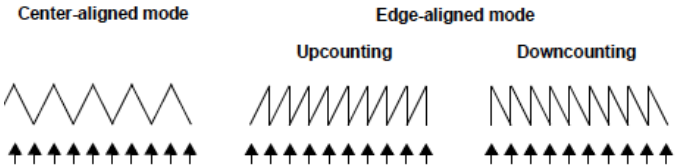


Center-aligned mode [1]

For Center-aligned mode, the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot 2 \cdot TIM\_ARR$$

For all modes, the timer model operates in preloaded mode, meaning that the used configuration is updated simultaneously to the update events. The Repetition Counter functionality is not supported in the model.



Events used for configuration update [1]

In other words, all input terminals of the model, except the *CCER* register, are sampled with the instants of the update events.

The timer mode, direction and output compare flag behavior can be set jointly using the *TIM_CR1* register.

Timer Mode Configuration

The *CKD* field only has an effect on the subtypes with PWM dead time generation and is therefore described in a later section. The register cell *CMS* can be used to determine the counter mode and the output compare flag behavior.

- 00 - Edge-aligned mode
- 01 - Center-aligned mode 1 - compare flags only set when counting down
- 10 - Center-aligned mode 2 - compare flags only set when counting up
- 11 - Center-aligned mode 3 - compare flags set when counting up and down

In Edge-aligned mode, the *DIR* bit determines the counter direction.

- 0 - Upcounting
- 1 - Downcounting

The module assumes the timer as always active and to be operated in preloaded mode with the update event generation always enabled. Therefore, the following settings are mandatory when using the register-based version.

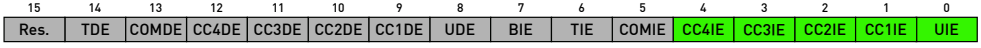
- TIM_CR1.ARPE = 1
- TIM_CR1.UDIS = 0
- TIM_CR1.CEN = 1

Initialization and Synchronization

The timer allows a counter initialization in the component mask. Further, the initial counter direction can be specified which only affects the Center-Aligned Mode. With a positive flank at the SYNC terminal, the counter is reset to zero and the dynamic configuration is updated. The initialization and synchronization features enable time-shifted pwm signals using multiple timer modules.

Interrupt Flags

The timer module can generate interrupt flags at the *CCxIF* and *UIF* output terminals. Those flags are based on the counter compare and update event flags and can be used in the model to, i.e., trigger an ADC conversion or a new control step via the PIL block. Note that in the model those flags are implemented as pulses.



Interrupt enable register

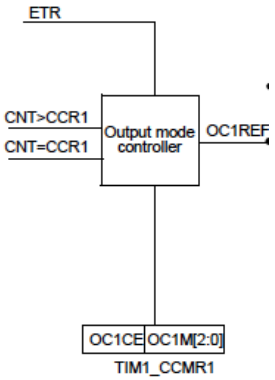
The interrupt flags can be enabled with the bits of the *TIM_DIER* register.

- 0 - interrupt disabled
- 1 - interrupt enabled

Note Only the four channel subtype implementations make use of all *CCxIE* fields.

Output Mode Controller

The output-mode controller generates up to 4 reference signals *OCyREF* based on the output compare flags of the counter.



Output Mode Controller for *OCyREF* [1]

The controller implements several output modes defining the behavior of *OCyREF*. With the register fields *TIM_CCMRx.OCyM*, the mode of each reference signal can be specified separately.

- 000 - Frozen, comparisons have no effect on *OCyREF*
- 001 - Active match mode, *OCyREF* forced high when $CTR = CCRy$
- 010 - Inactive match mode, *OCyREF* forced low when $CTR = CCRy$
- 011 - Toggle mode, *OCyREF* toggled when $CTR = CCRy$
- 100 - Force inactive mode, *OCyREF* always forced low
- 101 - Force active mode, *OCyREF* always forced high
- 110 - PWM Mode 1
- 111 - PWM Mode 2

Because the reference signal mode is supposed to be changed during simulation, the OCyM fields can be accessed via the input terminals. Note that those are also updated with the update events generated by the timer.

The hardware options to externally clear the reference signal are not supported in the model. Further, the break function of the timer is not part of the model assuming the flag *BDTR.MOE* is always set. Therefore it is mandatory to set *MOE* to 1 while using the resister-based version.

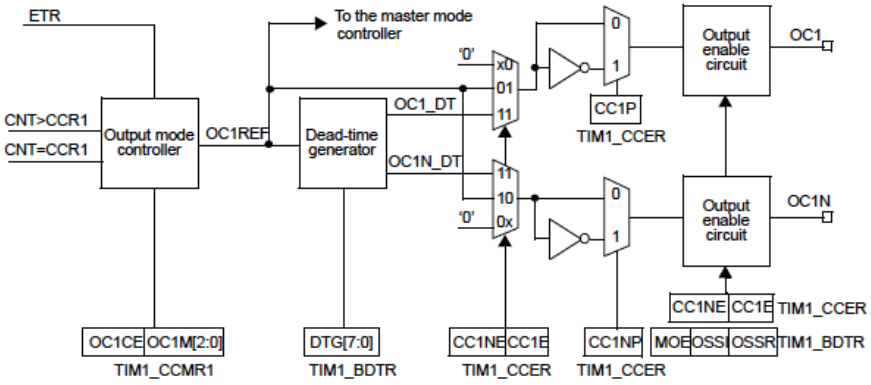
The options available in the output stage majorly depend on the timer subtype and therefore are discussed in the subsequent sections. The configuration of all output stages is done with the *CCER* register.

Note The *CCER* is accessed via the input terminals and is not preloaded. This means that a change on the *CCER* input directly effects the outputs.

---

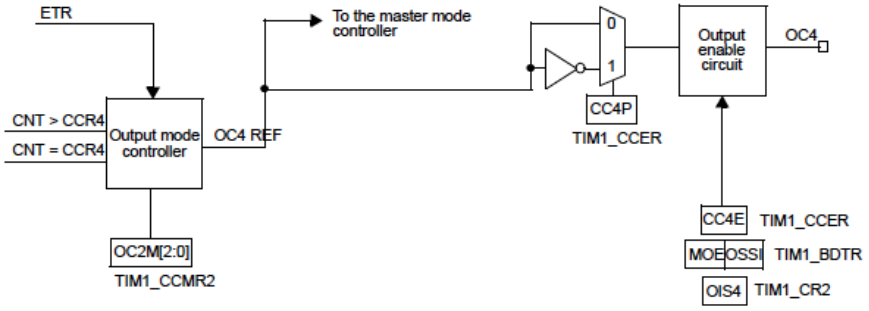
4 Channel Advanced Timer

The Advanced Timer consists of a timer and a 4 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned (up and down) as well as Center-aligned mode. For channels 1 to 3, the output stage enables complementary outputs with dead time and configurable polarity.



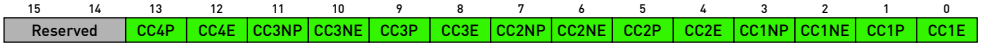
Output stage of Advanced Timer (channel 1 to 3) [1]

For channel 4, the output stage shown below only supports configurable polarity.



Output stage of Advanced Timer (channel 4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channels 1 to 3. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$

- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

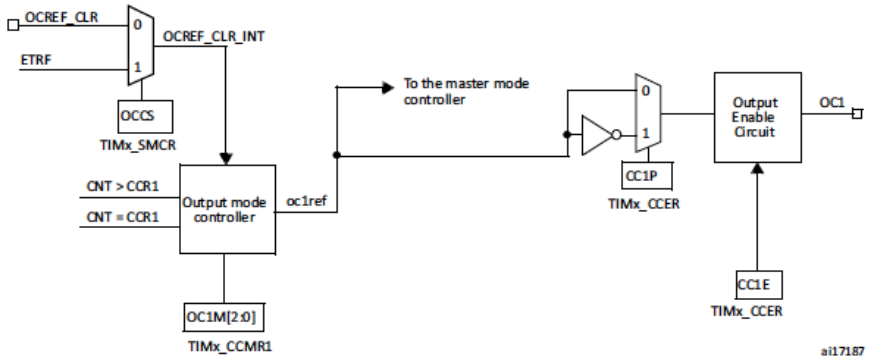
The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

This subtype implementation uses the full set of inputs, outputs and configuration registers.

4 Channel General Purpose Timer

This subtype is available with a 16-bit counter implementation supporting Edge-aligned (up and down), as well as Center-aligned modes. The 4 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.

15 14	13	12	11 10	9	8	7 6	5	4	3 2	1	0
Reserved	CC4P	CC4E	Reserved	CC3P	CC3E	Reserved	CC2P	CC2E	Reserved	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

The terminals used by this subtype are shown in the table below.

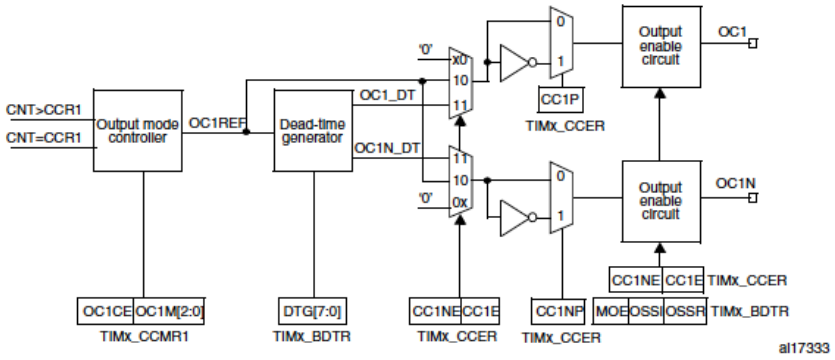
Terminal Group	Utilized	Unused
Input	CCR1 - CCR4, ARR, SYNC, OC1M - OC4M, CCER	x
Output	OC1 - OC4, CC1IF-CC4IF, UIF	OC1N - OC3N

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- GPIO Mode for unused outputs

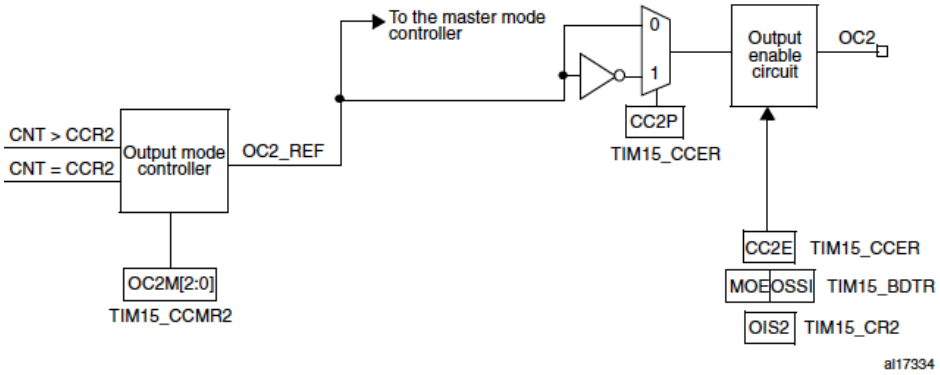
2 Channel Complementary GP Timer with Deadtime

This subtype consists of a timer and a 2 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned in upward direction. For channel 1 the output stage enables complementary outputs with dead time and configurable polarity.



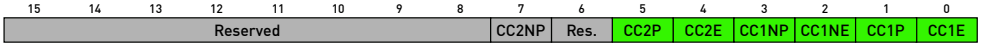
Output stage of Complementary GP Timer (channel 1) [1]

For channel 2, the output stage shown below only supports configurable polarity.



Output stage of Complementary GP Timer (channel 2) [1]

The *CCER* register can be used to configure the channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channel 1. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$

- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

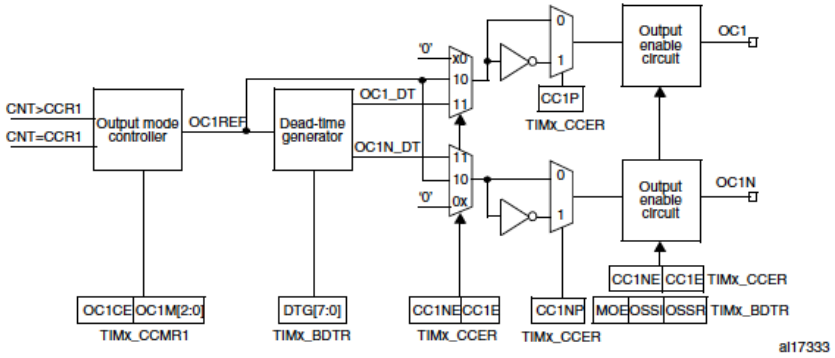
Terminal Group	Utilized	Unused
Input	CCR1 - CCR2, ARR, SYNC, OC1M - OC2M, CCER	CCR3 - CCR4, OC3M-OC4M
Output	OC1 - OC2, OC1N, CC1IF - CC2IF, UIF	OC3 - OC4, OC2N - OC3N, CC3IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC3IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel Complementary GP Timer with Deadtime

This subtype consists of a timer and a single channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned in upward direction. The output stage enables complementary outputs with dead time and configurable polarity on channel 1.



Output stage of Complementary GP Timer (channel 1) [1]

The *CCER* register can be used to configure the channels of the output stage separately.

Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channel 1. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

Dead time configuration

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

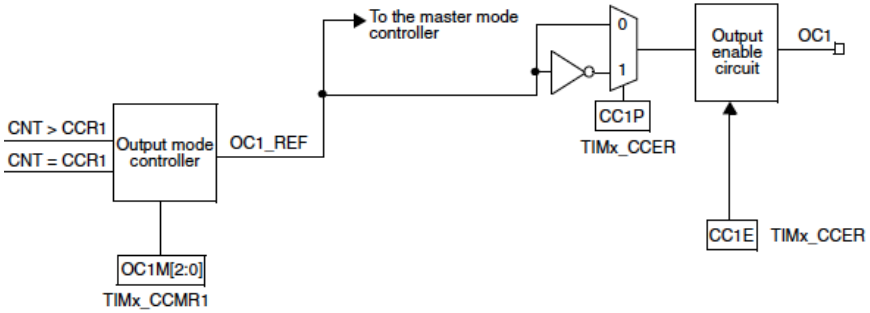
Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR4, OC2M-OC4M
Output	OC1, OC1N, CC1IF, UIF	OC2 - OC4, OC2N - OC3N, CC2IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

2 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The 2 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/2) [1]

The *CCER* register can be used to configure both channels of the output stage separately.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CC2NP	Res.	CC2P	CC2E	CC1NP	Res.	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CCxNP bits have no effect on the model.

The terminals used by this subtype are shown in the table below.

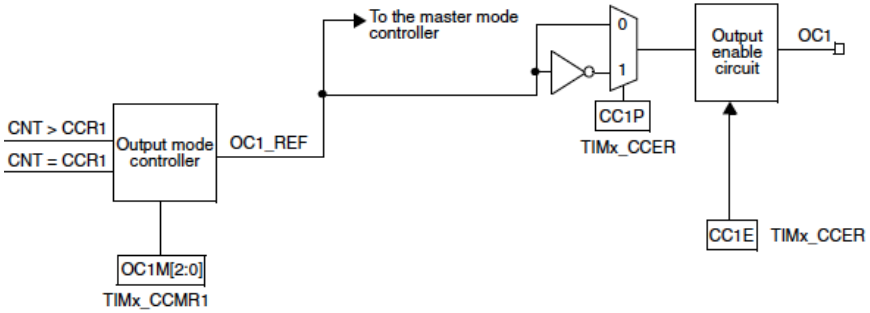
Terminal Group	Utilized	Unused
Input	CCR1 - CCR2, ARR, SYNC, OC1M - OC2M, CCER	CCR3 - CCR4, OC3M-OC4M
Output	OC1 - OC2, CC1IF - CC2IF, UIF	OC3 - OC4, OC1N - OC3N, CC3IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- TIM_DIER.CC3IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The single channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/1) [1]

The *CCER* register can be used to configure the single channel output stage.

Configuration of the output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CC1NP bit has no effect on the model.

The terminals used by this subtype are shown in the table below.

Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR4, OC2M-OC4M
Output	OC1, CC1IF, UIF	OC2 - OC4, OC1N - OC3N, CC2IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

GPIO Mode

In case that an output enable circuit is configured as inactive, the output level is determined by the GPIO Mode. To mimic this in the simulation model, the parameter GPIO Mode is available in the register-based version.

Configuration of GPIO Mode

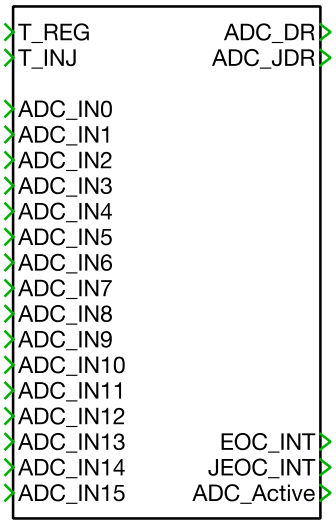
With the bits *OCx* and *OCxN*, the corresponding output mode can be set.

- 0 - Pull-Down (Inactive Low)
- 1 - Pull-Up (Inactive High)

Note This Register is available only in the simulation.

Analog-Digital Converter (ADC)

The PLECS peripheral library provides two blocks for the STM32 F1 ADC module, one with a register-based configuration mask and a second with a GUI. The figure below shows the appearance of the block.



ADC module model

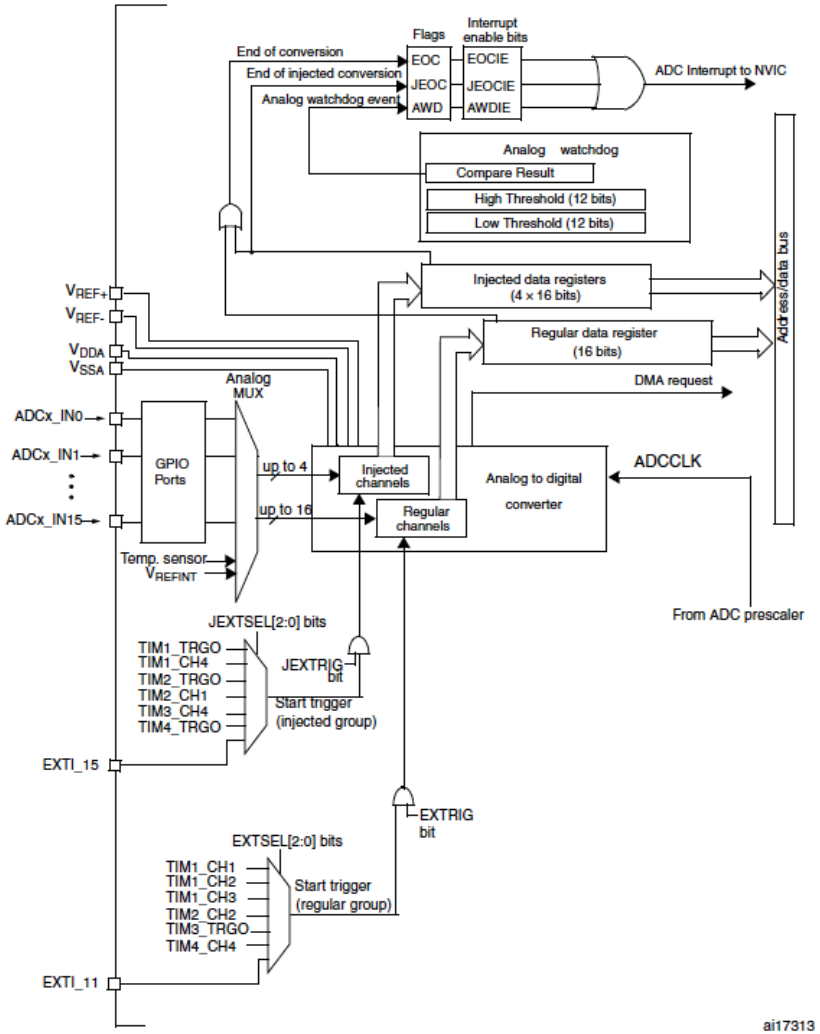
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *T_REG, T_INJ* - input ports to trigger ADC conversions
- *ADC_INx* - input measurement channels
- *ADC_DR* - auto-size output port to access regular conversion results
- *ADC_JDR* - auto-size output port to access injected conversion results
- *xEOC_INT* - output ports for subsequent logic triggered by a conversion end
- *ADC_Active* - output port indicating an active conversion

ADC Module Overview

The PLECS ADC model contains the most relevant features of the MCU peripheral.



Overview of the STM F1 ADC module [1]

The ADC model implements these logical submodules:

- ADC Converter with Result Registers for Injected and Regular conversion
- ADC Sample Logic for Single, Scan and Discontinuous mode
- ADC Interrupt Logic

For simplicity, the external trigger configuration shown in the figure above is neglected. The trigger to the regular and injected channels are directly accessed via the corresponding input terminals. Further, the Analog Watchdog functionalities as well as the Watchdog interrupt are not part of the model. Due to simulation efficiency reasons, the ADC can not be operated in continuous conversion mode.

ADC Converter with Result Registers

The ADC module contains a 12-bit converter. An external voltage reference is used which can be defined in the component mask.

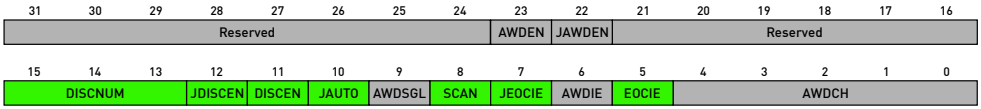
The period of the ADC clock, and therefore the time base for the module, can also be specified in the component mask.

For the regular channels, the hardware ADC contains a single 16-bit result register *ADC_DR*. The results of multiple, sequential regular group conversions are typically moved to the *SRAM* on the fly via the *DMA controller*. To simplify this, the *ADC_DR* terminal can provide the conversion result for each of the 16 regular group members separately. For the injected channels, the *ADC_JDR* terminal can provide access to the contents of all four *ADC_JDRx* registers. In the model, both result output ports are auto-sized. This means that their width is determined by the length of the regular or injected sequence.

The component only supports the right aligned result representation mode. In addition to this, the model provides an option to represent the conversion results as quantized double integers, which can be chosen with the mask parameter **Output Mode**.

ADC Sample Logic

The ADC model supports the single, scan and discontinuous conversion modes as well as auto-injected conversions. The continuous conversion mode is not supported due to simulation efficiency reasons. The *ADC_CR1* register can be used to choose and control the used conversion mode.



ADC_CR1 Register structure

The *DISCNUM* field defines the number of regular channels converted after a trigger to the regular group was received in discontinuous mode.

DISCNUM	Channels converted
000	1 channel
001	2 channels
...	...
110	7 channels
111	8 channels

The bit *JDISCEN* determines the discontinuous mode for injected channels:

- 0 - Discontinuous mode on injected channels disabled
- 1 - Discontinuous mode on injected channels enabled

With *DISCEN*, the discontinuous mode can be enabled for regular channels:

- 0 - Discontinuous mode on regular channels disabled
- 1 - Discontinuous mode on regular channels enabled

The bit *JAUTO* can be used to automatically trigger an injected group conversion after the regular group was finished:

- 0 - Automatic injected group conversion disabled
- 1 - Automatic injected group conversion enabled

Note Be aware that *JDISCEN* and *DISCEN* exclude each other and *JAUTO* can not be used with discontinuous mode or triggers to the injected group.

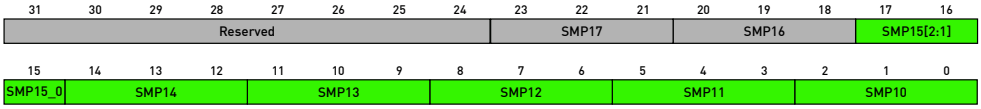
With the bit *SCAN*, the user can activate the scan mode of the component allowing multiple conversions triggered by a single event.

- 0 - Scan mode disabled
- 1 - Scan mode enabled

If none of the bits *JDISCEN*,*DISCEN* and *SCAN* is set, the adc module operates in single conversion mode. The bits *JEOCIE* and *EOCIE* are further described in the interrupt section.

For more information about the different conversion modes please refer to [2].

The sample time of a conversion can be configured separately for every analog input using the ADC SMPRx registers.

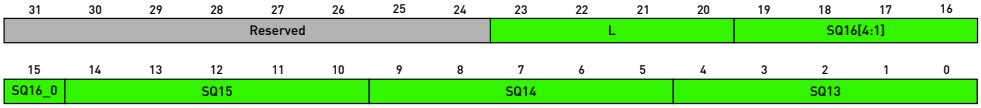


ADC_SMPRx Register structure

Note that *SMP16-SMP17* have no effect because the measurement options for the temperature sensor as well as the internal reference are not part of the model. For every other channel, the sampling time can be configured as follows:

SMPx	Sampling Time
000	1.5 cycles
001	7.5 cycles
010	13.5 cycles
011	28.5 cycles
100	41.5 cycles
101	55.5 cycles
110	71.5 cycles
111	239.5 cycles

The ADC operates as a sequencer which has a maximum sequence of 16 conversions for the regular group and 4 conversions for the injected group. The input sampled by each group element as well as the sequence length can be configured via the *ADC_SQRx* and the *ADC_JSQR* registers.



ADC_SQRx Register structure

The length of the regular sequence is defined by the field *L*.

L	Sequence length	Converted elements / ADC_DR
0000	1 conversion	[SQ1]
0001	2 conversion	[SQ1 SQ2]
...	...	...
1111	16 conversions	[SQ1 SQ2 ... SQ16]

ADC_JSQR Register structure

The length of the injected sequence is defined by the field *JL*.

JL	Sequence length	Converted elements / ADC_JDR
00	1 conversion	[JSQ4]
01	2 conversion	[JSQ3 JSQ4]
...	...	...
11	4 conversions	[JSQ1 JSQ2 JSQ3 JSQ4]

After the last conversion is finished, the sequencer wraps around and restarts with the first element after the next trigger was received.

For every sequence element, the sampled input can be specified via the corresponding *SQx* or *JSQx* fields as follows:

SQx/JSQx	Input
x0000	ADC_IN0
x0001	ADC_IN1
...	...
x1111	ADC_IN15

Note The terminals *ADC_DR* and *ADC_JDR* are auto-size output terminals. This means that the width of the terminals is defined by *J* or *JL* as shown in the upper tables.

ADC Interrupt Logic

The ADC module also has a connection to the *NVIC* of the *STM F1 MCU*. The *EOC* flag is set when either the regular channel or the injected channel indicates an end of conversion. The *JEOC* flag is set when the injected group indicates a finished conversion. The fields *ADC_CR1.EOCIE* and *ADC_CR1.JEOCIE* can be used to configure the adc to provide an interrupt pulse to the corresponding output terminals.

- 0 - no interrupt pulses are generated at the EOC_INT/JEOC_INT terminal
- 1 - interrupt pulses are generated at the EOC_INT/JEOC_INT terminal

Even if there typically won't be a model of the *NVIC* within the simulation, those pulses can i.e. be used to trigger the PIL block modeling a control step triggered by a finished adc conversion.

Reference

1 - Literature Source: STM32 Reference Manual [RM0041]

6

STM32 F3xx Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

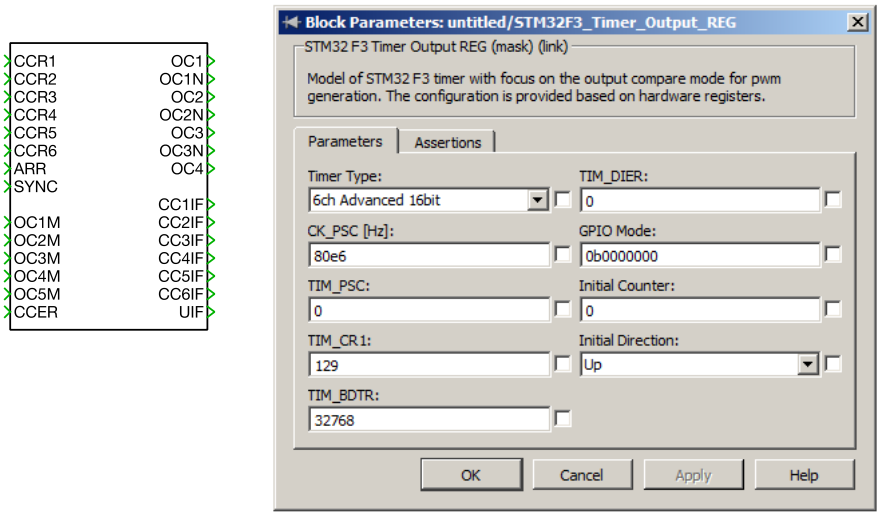
The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

System Timer for PWM Generation (Output Mode)

The PLECS peripheral library provides two blocks for the STM32 F3 system timer used in output mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer model for output mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Timer Subtypes

The STM32 F3 MCU's provide several subtypes of timers which can be used for input capture, output compare and PWM generation functionalities. In the presented model, all subtypes listed below are combined in one module and can be chosen via the component mask:

- 6 Channel 16bit Advanced Timer with Complementary Outputs
- 4 Channel 32bit General Purpose Timer
- 4 Channel 16bit General Purpose Timer
- 2 Channel 16bit GP Timer with Complementary Outputs
- 1 Channel 16bit GP Timer with Complementary Outputs

The focus of this model is the timer output behavior meaning that all input functionalities are disregarded. This corresponds to the hardware behavior with all TIM_CCMRx.CCyS cells being set to 00. Further, the One-Shot mode of the module is not supported. In the following sections, the common part of all subtypes is explained together with the models limitations. Further, the differences between the subtypes are described in more detail.

General Counter Behavior

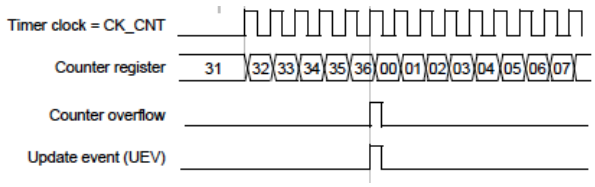
The base of all timer modules is an auto-reload counter driven by a prescaled counter clock *CK_CNT*. The period of this time base clock is determined by the counter clock frequency *CK_PSC* and the prescaler register *TIM_PSC*, both configurable in the mask, as follows:

$$T_{CK\_CNT} = \frac{TIM\_PSC + 1}{CK\_PSC}$$

The counter either operates in Edge-aligned mode with configurable direction or in Center-aligned mode. In addition to the general counter functionality, the module also generates output compare interrupt flags when the counter matches the values stored in the *CCRx* registers. Those flags are later used to determine the output levels of the timer module.

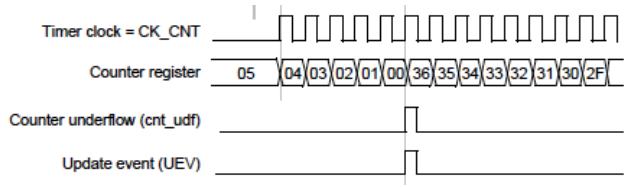
Edge-aligned mode

In upcounting direction, the counter counts from 0 to the counter period value *TIM_ARR* and generates an update event *UEV* simultaneous to the counter overflow.



Edge-aligned mode / Upcounting [1]

In downcounting direction, the counter counts from *TIM_ARR* to 0 and generates an update event (*UEV*) simultaneous to the counter underflow.



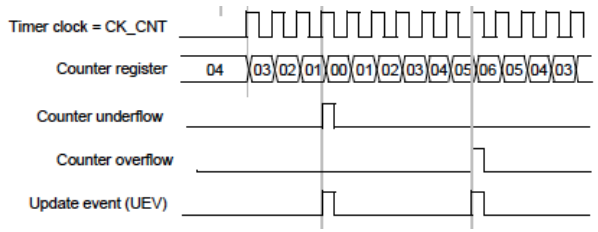
Edge-aligned mode / Downcounting [1]

In Edge-aligned mode, the counter period and therefore the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot (TIM\_ARR + 1)$$

Center-aligned mode

In this mode, the counter alternates its direction and generates an update event (*UEV*) at the counter under- and overflow.

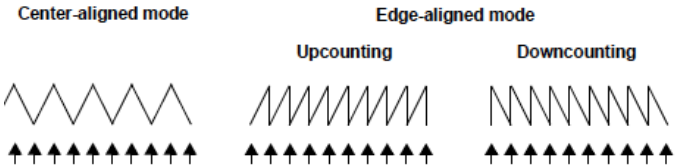


Center-aligned mode [1]

For Center-aligned mode, the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot 2 \cdot TIM\_ARR$$

For all modes, the timer model operates in preloaded mode, meaning that the used configuration is updated simultaneously to the update events. The Repetition Counter functionality is not supported in the model.



Events used for configuration update [1]

In other words, all input terminals of the model, except the *CCER* register, are sampled with the instants of the update events.

The timer mode, direction and output compare flag behavior can be set jointly using the *TIM_CR1* register.

Timer Mode Configuration

The *CKD* field only has an effect on the subtypes with PWM dead time generation and is therefore described in a later section. The register cell *CMS* can be used to determine the counter mode and the output compare flag behavior.

- 00 - Edge-aligned mode
- 01 - Center-aligned mode 1 - compare flags only set when counting down
- 10 - Center-aligned mode 2 - compare flags only set when counting up
- 11 - Center-aligned mode 3 - compare flags set when counting up and down

In Edge-aligned mode, the *DIR* bit determines the counter direction.

- 0 - Upcounting
- 1 - Downcounting

The module assumes the timer as always active and to be operated in preloaded mode with the update event generation always enabled. Therefore, the following settings are mandatory when using the register-based version.

- TIM_CR1.ARPE = 1
- TIM_CR1.UDIS = 0
- TIM_CR1.CEN = 1

Initialization and Synchronization

The timer allows a counter initialization in the component mask. Further, the initial counter direction can be specified which only affects the Center-Aligned Mode. With a positive flank at the SYNC terminal, the counter is reset to zero and the dynamic configuration is updated. The initialization and synchronization features enable time-shifted pwm signals using multiple timer modules.

Interrupt Flags

The timer module can generate interrupt flags at the *CCxIF* and *UIF* output terminals. Those flags are based on the counter compare and update event flags and can be used in the model to, i.e., trigger an ADC conversion or a new control step via the PIL block. Note that in the model those flags are implemented as pulses.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	TDE	COMDE	CC4DE	CC3DE	CC2DE	CC1DE	UDE	BIE	TIE	COMIE	CC4IE	CC3IE	CC2IE	CC1IE	UIE

Interrupt enable register

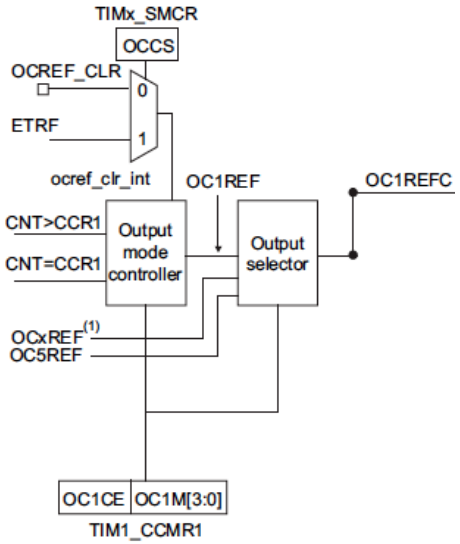
The interrupt flags can be enabled with the bits of the *TIM_DIER* register.

- 0 - interrupt disabled
- 1 - interrupt enabled

Note Only the four channel subtype implementations make use of all *CCxIE* fields. Channel 5 & 6 have no field in *TIM_DIER* and therefore are assumed to be always active.

Output Mode Controller and Output Selector

The output-mode controller generates up to 4 reference signals *OCyREF* based on the output compare flags of the counter.



Output Mode Controller and Output Selector for *OCyREFC* [1]

The Output selector enables Asymmetric and Combined PWM Modes. With the register fields *TIM_CCMRx.OCyM*, the behavior of each *OCyREF*/*OCyREFC* signal can be specified separately.

- 0000 - Frozen, comparisons have no effect on *OCyREF*
- 0001 - Active match mode, *OCyREF* forced high when $CTR = CCRy$
- 0010 - Inactive match mode, *OCyREF* forced low when $CTR = CCRy$
- 0011 - Toggle mode, *OCyREF* toggled when $CTR = CCRy$
- 0100 - Force inactive mode, *OCyREF* always forced low
- 0101 - Force active mode, *OCyREF* always forced high
- 0110 - PWM Mode 1
- 0111 - PWM Mode 2
- 1000 - Not supported
- 1001 - Not supported

- 1010 - Not supported
- 1011 - Not supported
- 1100 - Combined PWM Mode 1
- 1101 - Combined PWM Mode 2
- 1110 - Asymmetric PWM Mode 1
- 1111 - Asymmetric PWM Mode 2

Because the signal mode is supposed to be changed during simulation, the OCyM fields can be accessed via the input terminals. Note that those are also updated with the update events generated by the timer.

For the 6ch Advanced Timer module there is also a Combined 3-phase PWM mode available which is depending on *OC5REF*. For more details regarding the different modes see [1].

The hardware options to externally clear the reference signal are not supported in the model. Further, the break function of the timer is not part of the model assuming the flag *BDTR.MOE* is always set. Therefore it is mandatory to set *MOE* to 1 while using the resister-based version.

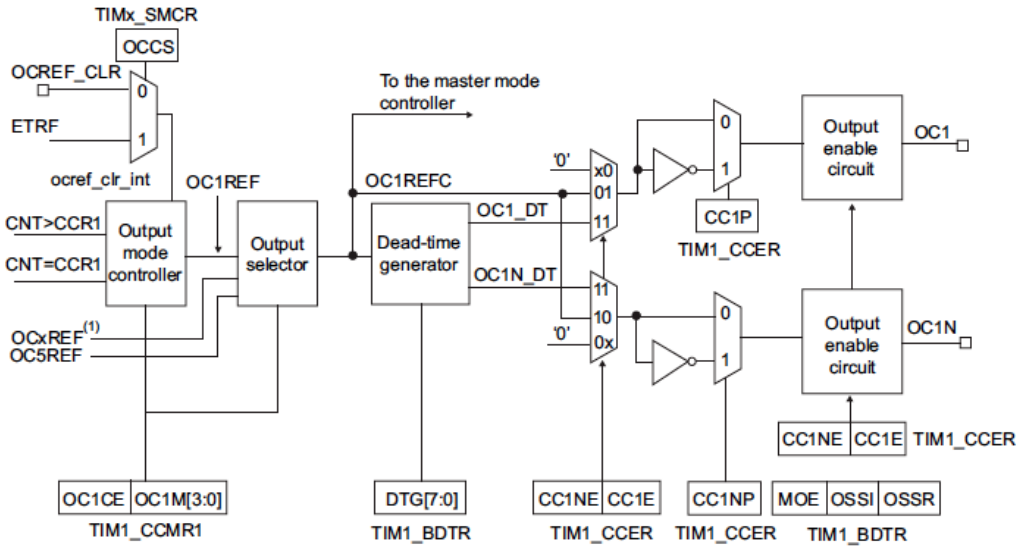
The options available in the output stage majorly depend on the timer subtype and therefore are discussed in the subsequent sections. The configuration of all output stages is done with the *CCER* register.

Note The *CCER* is accessed via the input terminals and is not preloaded. This means that a change on the *CCER* input directly effects the outputs.

---

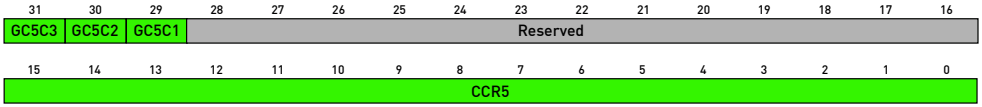
6 Channel Advanced Timer

The Advanced Timer consists of a timer and a 6 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned (up and down) as well as Center-aligned mode. Because the channels 5 and 6 are not connected to the pins of the MCU, the outputs are not available in the peripheral model. However, the signals produced by stage 5 and 6 are used internally. For channels 1 to 3, the output stage enables complementary outputs with dead time and configurable polarity.



Output stage of Advanced Timer (channel 1 to 3) [1]

The advanced timer enables a Combined 3-phase PWM Mode which is controlled by the *GC5Cx* bits located in the *CCR5* register.



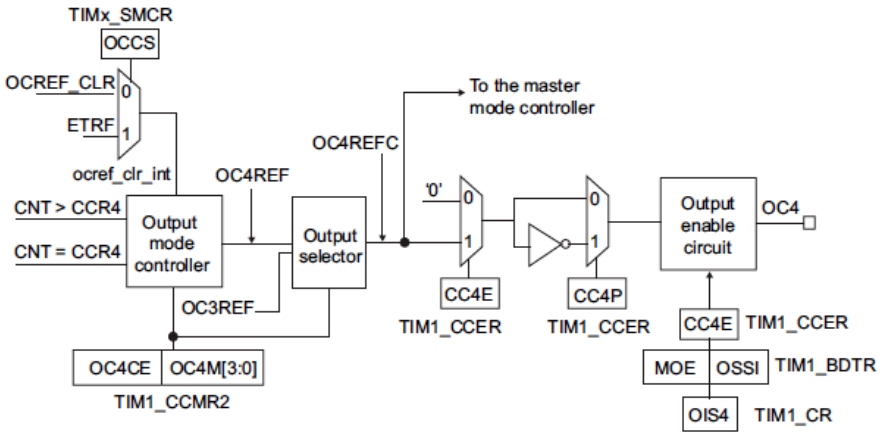
Channel-wise configuration of output stage

The signal *OC5REF* has the following effect on *OCxREFC* for *GC5Cx*.

- 0 - No effect of *OC5REF* on *OCxREFC*
- 1 - *OCxREFC* is the logical and between *OCxREFC* and *OC5REF*

Note *CCR5* is part of the dynamic configuration and therefore can be accessed via the input.

For channel 4, the output stage only supports configurable polarity.



Output stage of Advanced Timer (channel 4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CC6P	CC6E	Res.	Res.	CC5P	CC5E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4NP	Res.	CC4P	CC4E	CC3NP	CC3NE	CC3P	CC3E	CC2NP	CC2NE	CC2P	CC2E	CC1NP	CC1NE	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREFC
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channels 1 to 3. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREFC, OCxN inactive
1	0	OCx inactive, OCxN = OCxREFC
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

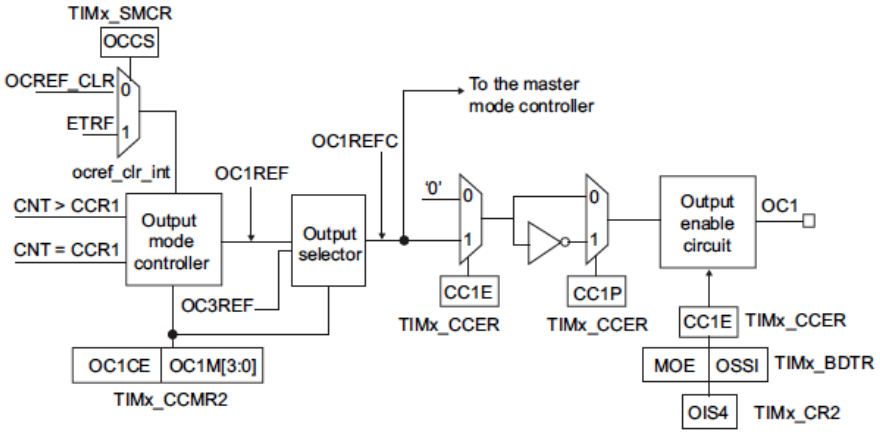
The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

This subtype implementation uses the full set of inputs, outputs and configuration registers.

4 Channel General Purpose Timer

This subtype is available with a 16-bit or 32-bit counter implementation both supporting Edge-aligned (up and down), as well as Center-aligned modes. The 4 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CC6P	CC6E	Res.	Res.	CC5P	CC5E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4NP	Res.	CC4P	CC4E	CC3NP	CC3NE	CC3P	CC3E	CC2NP	CC2NE	CC2P	CC2E	CC1NP	CC1NE	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREFC
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CCxNP bits have no effect on the model.

The terminals used by this subtype are shown in the table below.

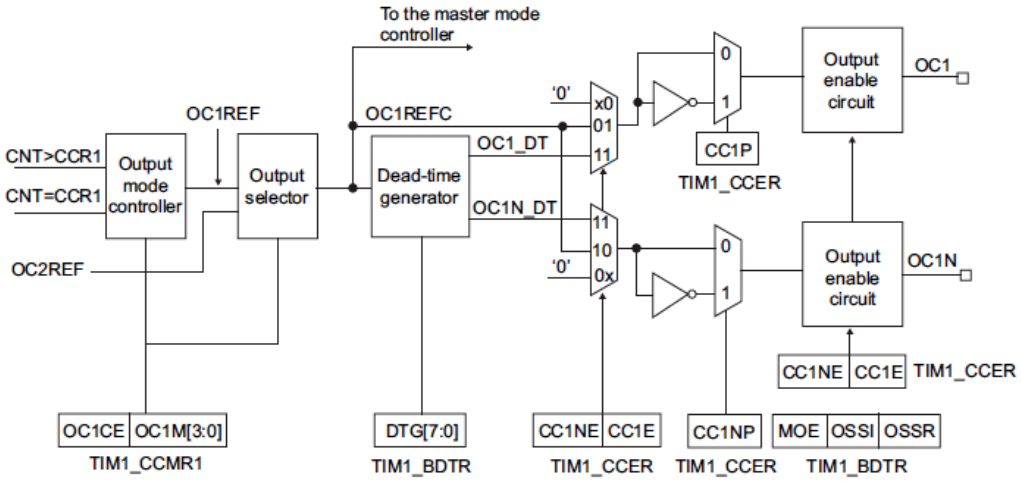
Terminal Group	Utilized	Unused
Input	CCR1 - CCR4, ARR, SYNC, OC1M - OC4M, CCER	OC5M, CCR5, CCR6
Output	OC1 - OC4, CC1IF - CC4IF, UIF	OC1N - OC3N, CC5IF, CC6IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- GPIO Mode for unused outputs

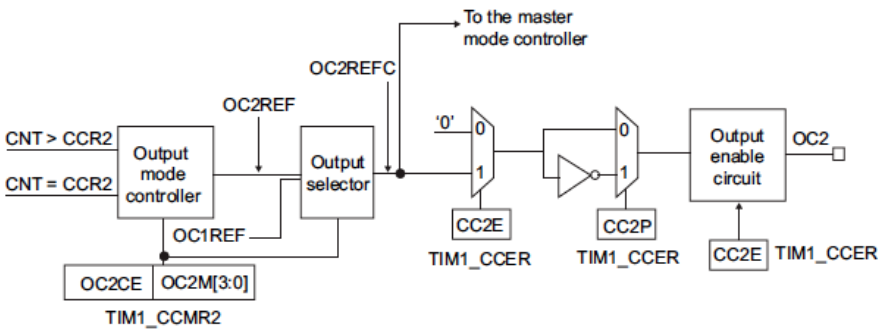
2 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. Channel 1 of the output stage supports complementary outputs with dead time and configurable polarity.



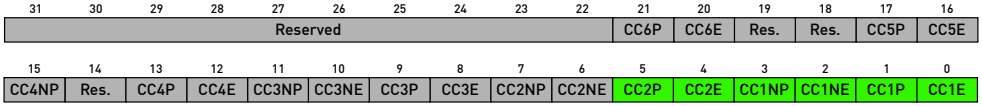
Output stage of general purpose timer channel 1 [1]

Channel 2 of the output stage only supports configurable polarity.



Output stage of general purpose timer channel 2 [1]

The *CCER* register can be used to configure both channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREFC
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channel 1. The table below shows this for both outputs operated with equal polarity.

CC1NE	CC1E	Behavior
0	0	OC1 & OC1N inactive
0	1	OC1 = OC1REFC, OC1N inactive
1	0	OC1 inactive, OC1N = OC1REFC
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OC1* and *OC1N* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$

- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

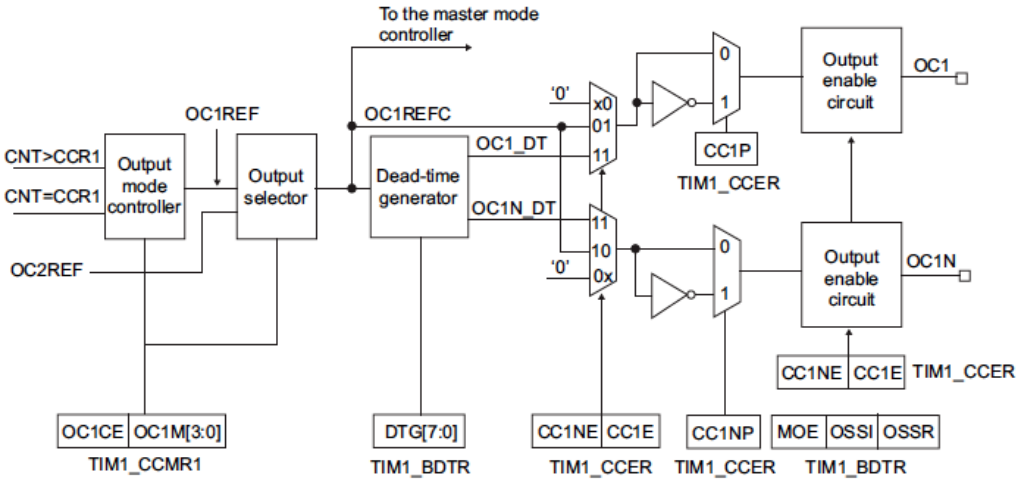
Terminal Group	Utilized	Unused
Input	CCR1 - CCR2, ARR, SYNC, OC1M - OC2M, CCER	CCR3 - CCR6, OC3M-OC5M
Output	OC1 - OC2, OC1N, CC1IF - CC2IF, UIF	OC3 - OC4, OC2N - OC3N, CC3IF - CC6IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC3IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The single channel output stage supports complementary outputs with dead time and configurable polarity.



Output stage of general purpose timer channel [1]

The *CCER* register can be used to configure the single channel output stage.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved										CC6P	CC6E	Res.	Res.	CC5P	CC5E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4NP	Res.	CC4P	CC4E	CC3NP	CC3NE	CC3P	CC3E	CC2NP	CC2NE	CC2P	CC2E	CC1NP	CC1NE	CC1P	CC1E

Configuration of the output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREFC

- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior. The table below shows this for both outputs operated with equal polarity.

CC1NE	CC1E	Behavior
0	0	OC1 & OC1N inactive
0	1	OC1 = OC1REFC, OC1N inactive
1	0	OC1 inactive, OC1N = OC1REFC
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OC1* and *OC1N* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

The terminals used by this subtype are shown in the table below.

Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR6, OC2M-OC5M
Output	OC1, OC1N, CC1IF, UIF	OC2 - OC4, OC2N - OC3N, CC2IF - CC6IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

GPIO Mode

In case that an output enable circuit is configured as inactive, the output level is determined by the GPIO Mode. To mimic this in the simulation model, the parameter GPIO Mode is available in the register-based version.

Configuration of GPIO Mode

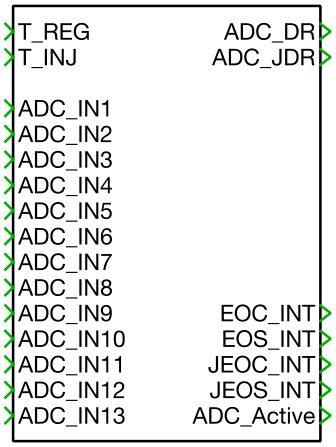
With the bits *OCx* and *OCxN*, the corresponding output mode can be set.

- 0 - Pull-Down (Inactive Low)
- 1 - Pull-Up (Inactive High)

Note This Register is available only in the simulation.

Analog-Digital Converter (ADC)

The PLECS peripheral library provides two blocks for the STM32 F3 single mode ADC module, one with a register-based configuration mask and a second with a GUI. The figure below shows the appearance of the block.



ADC module model

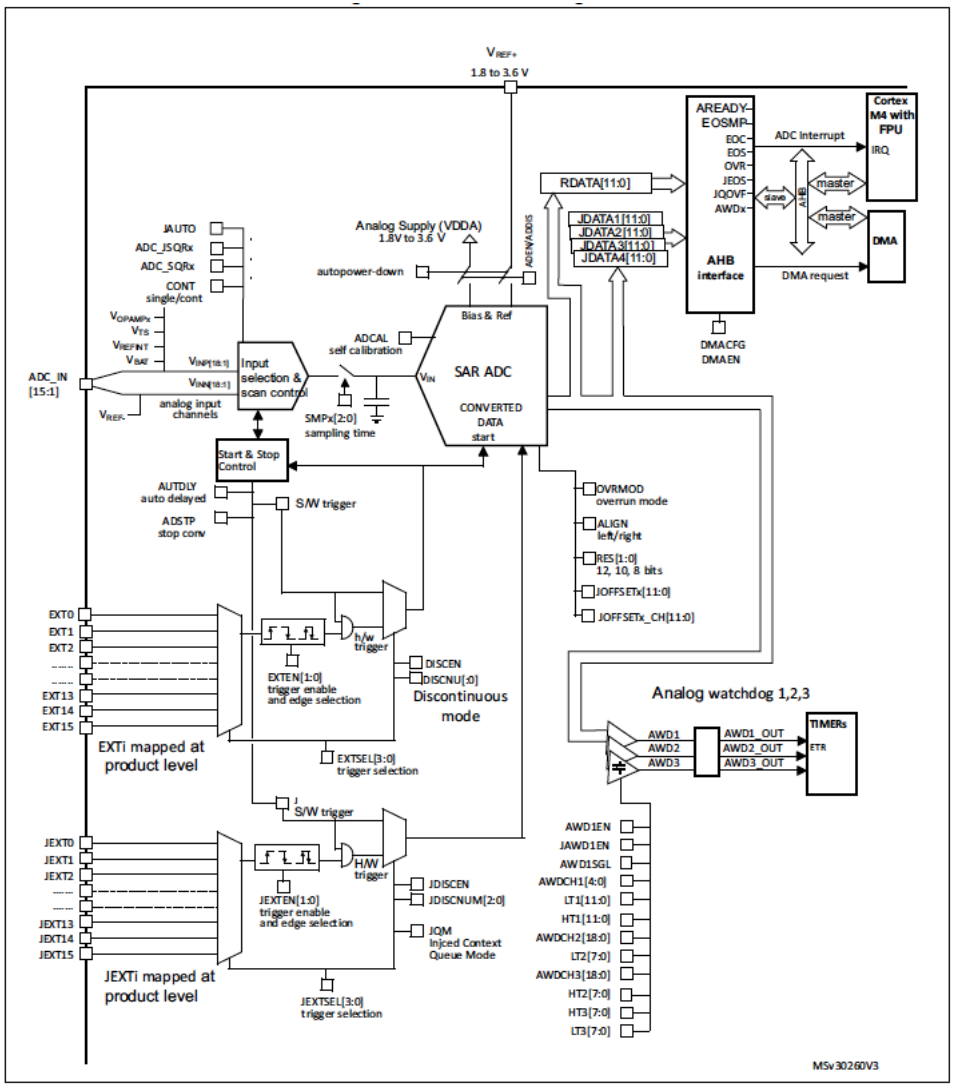
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *T_REG, T_INJ* - input ports to trigger ADC conversions
- *ADC_INx* - input measurement channels
- *ADC_DR* - auto-size output port to access regular conversion results
- *ADC_JDR* - auto-size output port to access injected conversion results
- *xEOC_INT* - output ports for subsequent logic triggered by a conversion end
- *xEOS_INT* - output ports for subsequent logic triggered by a sequence end
- *ADC_Active* - output port indicating an active conversion

ADC Module Overview

The PLECS single ADC model contains the most relevant features of the MCU peripheral.



Overview of the STM F3 ADC module [1]

The ADC model implements these logical submodules:

- ADC Converter supporting Single-ended and Differential mode
- Result Registers for Injected and Regular conversion
- ADC Sample Logic for Single and Discontinuous mode
- ADC Interrupt Logic

For simplicity, the external trigger configuration shown in the figure above is neglected. The trigger to the regular and injected channels are directly accessed via the corresponding input terminals. This can also be used to model software triggered conversions. Further, the Analog Watchdog functionalities, the Watchdog and DMA overrun interrupts as well as the offset calculation are not part of the model. Stopping an ongoing conversion is either not supported. Due to simulation efficiency reasons, the ADC can not be operated in continuous conversion mode.

ADC Converter with Result Registers

The ADC module contains a converter with configurable resolution. An external voltage reference is used which, as well as the ADC clock, is a parameter of the component mask.

The resolution of the converter is set with the field *RES* of the *ADC_CFGR* register given in the next section. This also influences the amount of ADC clock cycles needed for a conversion. With the *RES* bits the resolution can be specified as shown in the table below.

RES[1]	RES[0]	Resolution	Conversion length
0	0	12 bit	12.5 ADCCLK cycles
0	1	10 bit	10.5 ADCCLK cycles
1	0	8 bit	8.5 ADCCLK cycles
1	1	6 bit	6.5 ADCCLK cycles

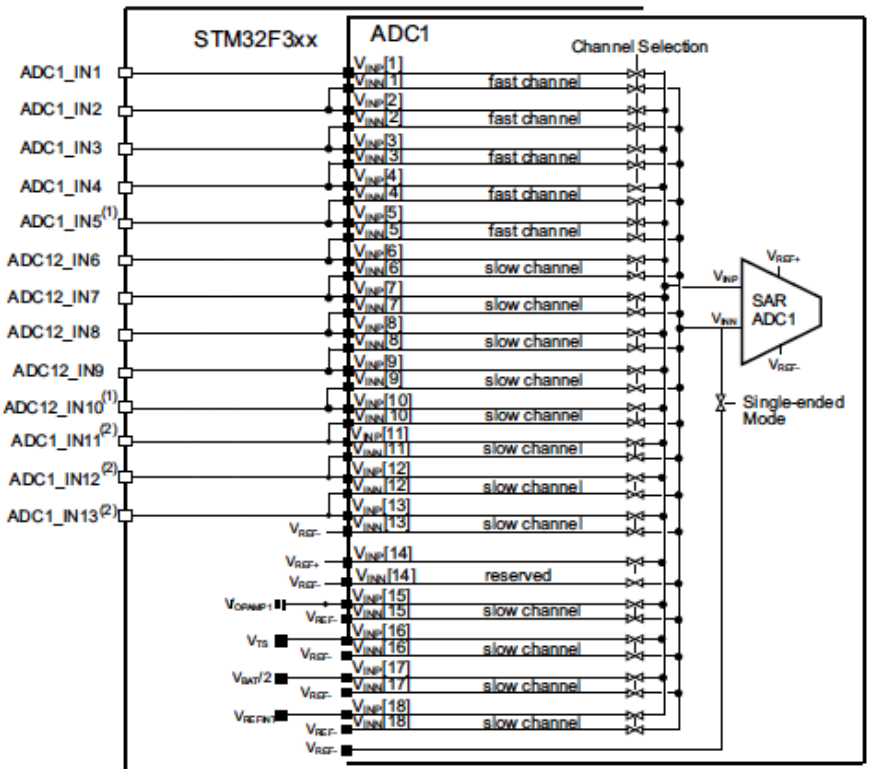
For the regular channels, the hardware ADC contains a single 16-bit result register *ADC_DR*. The results of multiple, sequential regular group conversions are typically moved to the *SRAM* on the fly via the *DMA controller*. To simplify this, the *ADC_DR* terminal can provide the conversion result for each of the 16 regular group members separately. For the injected channels, the *ADC_JDR* terminal can provide access to the contents of all four *ADC_JDRx*

registers. In the model, both result output ports are auto-sized. This means that their width is determined by the length of the regular or injected sequence.

The component only supports the right aligned result representation mode meaning that *ADC_CFGR.ALIGN* always needs to be set to 0. In addition to this, the model provides an option to represent the conversion results as quantized double integers, which can be chosen with the mask parameter **Output Mode**.

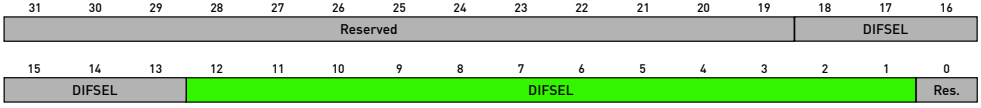
ADC Sample Logic

The ADC converter can be used for differential and single-ended conversions as indicated in the figure below.



Channel selection of the STM F3 ADC module [1]

The *DIFSEL* register defines if a channel is used in single-ended or differential mode.



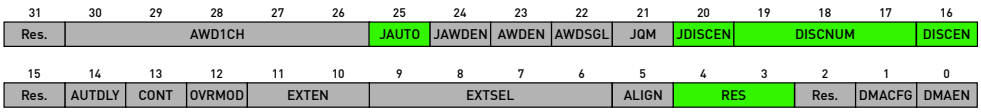
ADC_DIFSEL Register structure

Bit *i* of the register sets the mode of channel *i*.

- 0 - ADC analog input channel-i is configured in single-ended mode
- 1 - ADC analog input channel-i is configured in differential mode

By setting a channel to differential, channel *i+1* automatically acts as the negative input for the conversion. Consequently, channel *i+1* cannot be used for a normal conversion anymore and therefore is not allowed to be part of the regular nor the injected group.

The ADC model supports the single and discontinuous conversion modes as well as auto-injected conversions. The continuous conversion mode is not supported due to simulation efficiency reasons. The *ADC_CFGR* register is available to control the ADC conversion mode.



ADC_CFGR Register structure

The bit *JAUTO* is used to automatically trigger an injected group conversion after the regular group was finished:

- 0 - Automatic injected group conversion disabled
- 1 - Automatic injected group conversion enabled

The bit *JDISCEN* determines the discontinuous mode for injected channels:

- 0 - Discontinuous mode on injected channels disabled
- 1 - Discontinuous mode on injected channels enabled

The *DISCNUM* field defines the number of regular channels converted after a trigger to the regular group was received in discontinuous mode.

DISCNUM	Channels converted
000	1 channel
001	2 channels
...	...
110	7 channels
111	8 channels

With *DISCEN*, the discontinuous mode can be enabled for regular channels:

- 0 - Discontinuous mode on regular channels disabled
- 1 - Discontinuous mode on regular channels enabled

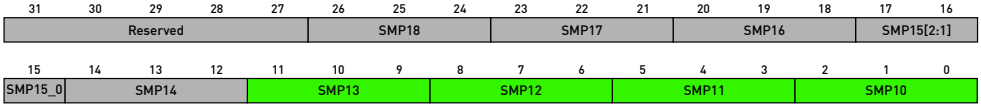
Note Be aware that *JDISCEN* and *DISCEN* exclude each other and *JAUTO* can not be used with discontinuous mode or triggers to the injected group.

If none of the bits *JDISCEN* and *DISCEN* is set, the adc module operates in single conversion mode.

For more information about the different conversion modes please refer to [1].

Note The adc model assumes the adc not to operate in continuous conversion mode and to be always active. Therefore *ADC_CFGR.CONT* needs to be cleared while using the register-based configuration.

For every analog input, the sample time of a conversion can be configured separately using the ADC SMPRx registers.

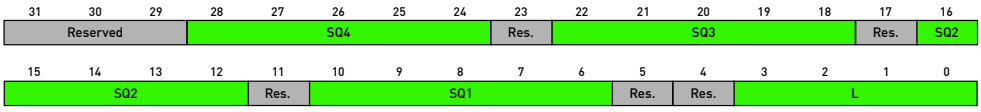


ADC_SMPRx Register structure

For channels 1 to 13, the sample time can be set as follows:

SMPx	Sample Time
000	1.5 cycles
001	2.5 cycles
010	4.5 cycles
011	7.5 cycles
100	19.5 cycles
101	61.5 cycles
110	181.5 cycles
111	601.5 cycles

The ADC operates as a sequencer which has a maximum sequence of 16 conversions for the regular group and 4 conversions for the injected group. The input sampled by each group element as well as the sequence length can be configured via the *ADC_SQRx* and the *ADC_JSQR* registers.



ADC_SQRx Register structure

The length of the regular sequence is defined by the field *L*.

L	Sequence length	Converted elements / ADC_DR
0000	1 conversion	[SQ1]
0001	2 conversion	[SQ1 SQ2]
...	...	...
1111	16 conversions	[SQ1 SQ2 ... SQ16]

ADC_JSQR Register structure

The length of the injected sequence is defined by the field *JL*.

JL	Sequence length	Converted elements / ADC_JDR
00	1 conversion	[JSQ1]
01	2 conversion	[JSQ1 JSQ2]
...	...	...
11	4 conversions	[JSQ1 JSQ2 JSQ3 JSQ4]

After the last conversion is finished, the sequencer wraps around and restarts with the first element after the next trigger was received.

For every sequence element, the sampled input can be specified via the corresponding *SQx* or *JSQx* fields as follows:

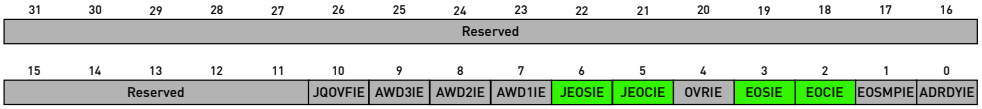
SQx/JSQx	Input
x0001	ADC_IN1
x0010	ADC_IN2
...	...
x1101	ADC_IN13

Note The terminals *ADC_DR* and *ADC_JDR* are auto-size output terminals. This means that the width of the terminals is defined by *J* or *JL* as shown in the upper tables.

ADC Interrupt Logic

The ADC module also has a connection to the *NVIC* of the *STM F3 MCU*. The model therefore provides the relevant flags at the output to be used in the simulation.

The register *ADC_IER* can be used to define which flags are set during operation.



ADC_IER Register structure

Reference

1 - Literature Source: STM32 Reference Manual [RM0316]

7

STM32 F2xx/F4xx Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical

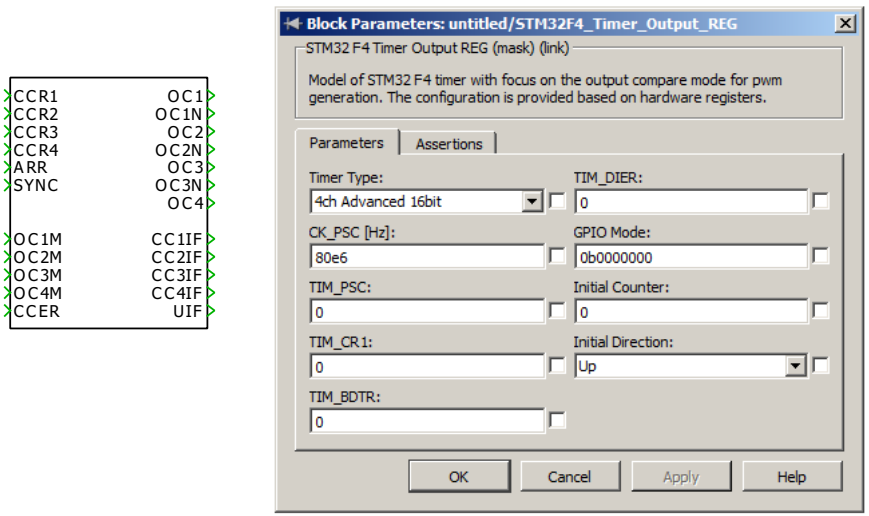
user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

System Timer for PWM Generation (Output Mode)

The PLECS peripheral library provides two blocks for the STM32 F2/F4 system timer used in output mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer model for output mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Timer Subtypes

The STM32 F2/F4 MCU's provide several subtypes of timers which can be used for input capture, output compare and PWM generation functionalities. In the presented model, all subtypes listed below are combined in one module and can be chosen via the component mask:

- 4 Channel 16bit Advanced Timer
- 4 Channel 32bit General Purpose Timer
- 4 Channel 16bit General Purpose Timer
- 2 Channel 16bit General Purpose Timer
- 1 Channel 16bit General Purpose Timer

The focus of this model is the timer output behavior meaning that all input functionalities are disregarded. This corresponds to the hardware behavior with all TIM_CCMRx.CCyS cells being set to 00. Further, the One-Shot mode of the module is not supported. In the following sections, the common part of all subtypes is explained together with the models limitations. Further, the differences between the subtypes are described in more detail.

General Counter Behavior

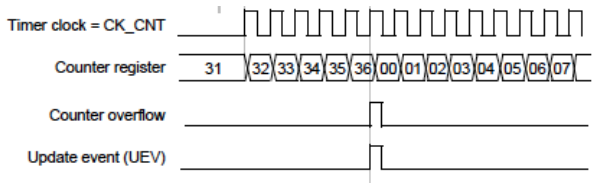
The base of all timer modules is an auto-reload counter driven by a prescaled counter clock *CK_CNT*. The period of this time base clock is determined by the counter clock frequency *CK_PSC* and the prescaler register *TIM_PSC*, both configurable in the mask, as follows:

$$T_{CK\_CNT} = \frac{TIM\_PSC + 1}{CK\_PSC}$$

The counter either operates in Edge-aligned mode with configurable direction or in Center-aligned mode. In addition to the general counter functionality, the module also generates output compare interrupt flags when the counter matches the values stored in the *CCRx* registers. Those flags are later used to determine the output levels of the timer module.

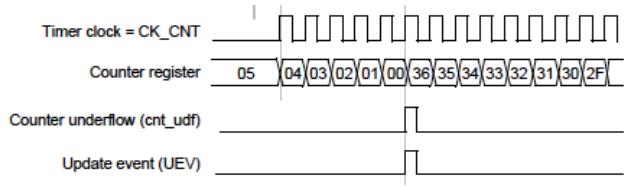
Edge-aligned mode

In upcounting direction, the counter counts from 0 to the counter period value *TIM_ARR* and generates an update event *UEV* simultaneous to the counter overflow.



Edge-aligned mode / Upcounting [1]

In downcounting direction, the counter counts from *TIM_ARR* to 0 and generates an update event (*UEV*) simultaneous to the counter underflow.



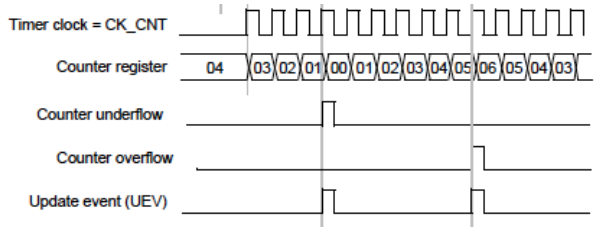
Edge-aligned mode / Downcounting [1]

In Edge-aligned mode, the counter period and therefore the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot (TIM\_ARR + 1)$$

Center-aligned mode

In this mode, the counter alternates its direction and generates an update event (*UEV*) at the counter under- and overflow.

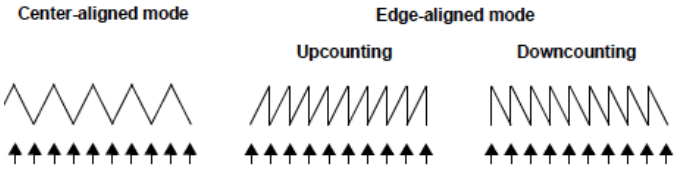


Center-aligned mode [1]

For Center-aligned mode, the PWM period is calculated as:

$$T_{PWM} = T_{CK\_CNT} \cdot 2 \cdot TIM\_ARR$$

For all modes, the timer model operates in preloaded mode, meaning that the used configuration is updated simultaneously to the update events. The Repetition Counter functionality is not supported in the model.



Events used for configuration update [1]

In other words, all input terminals of the model, except the *CCER* register, are sampled with the instants of the update events.

The timer mode, direction and output compare flag behavior can be set jointly using the *TIM_CR1* register.

Timer Mode Configuration

The *CKD* field only has an effect on the subtypes with PWM dead time generation and is therefore described in a later section. The register cell *CMS* can be used to determine the counter mode and the output compare flag behavior.

- 00 - Edge-aligned mode
- 01 - Center-aligned mode 1 - compare flags only set when counting down
- 10 - Center-aligned mode 2 - compare flags only set when counting up
- 11 - Center-aligned mode 3 - compare flags set when counting up and down

In Edge-aligned mode, the *DIR* bit determines the counter direction.

- 0 - Upcounting
- 1 - Downcounting

The module assumes the timer as always active and to be operated in preloaded mode with the update event generation always enabled. Therefore, the following settings are mandatory when using the register-based version.

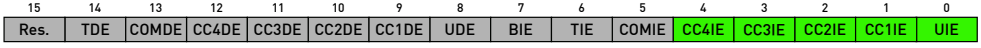
- TIM_CR1.ARPE = 1
- TIM_CR1.UDIS = 0
- TIM_CR1.CEN = 1

Initialization and Synchronization

The timer allows a counter initialization in the component mask. Further, the initial counter direction can be specified which only affects the Center-Aligned Mode. With a positive flank at the SYNC terminal, the counter is reset to zero and the dynamic configuration is updated. The initialization and synchronization features enable time-shifted pwm signals using multiple timer modules.

Interrupt Flags

The timer module can generate interrupt flags at the *CCxIF* and *UIF* output terminals. Those flags are based on the counter compare and update event flags and can be used in the model to, i.e., trigger an ADC conversion or a new control step via the PIL block. Note that in the model those flags are implemented as pulses.



Interrupt enable register

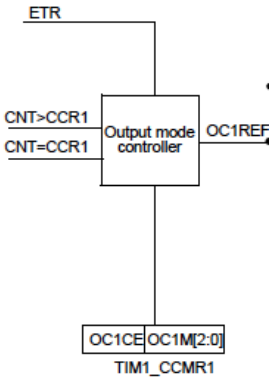
The interrupt flags can be enabled with the bits of the *TIM_DIER* register.

- 0 - interrupt disabled
- 1 - interrupt enabled

Note Only the four channel subtype implementations make use of all *CCxIE* fields.

Output Mode Controller

The output-mode controller generates up to 4 reference signals *OCyREF* based on the output compare flags of the counter.



Output Mode Controller for *OCyREF* [1]

The controller implements several output modes defining the behavior of *OCyREF*. With the register fields *TIM_CCMRx.OCyM*, the mode of each reference signal can be specified separately.

- 000 - Frozen, comparisons have no effect on *OCyREF*
- 001 - Active match mode, *OCyREF* forced high when $CTR = CCRy$
- 010 - Inactive match mode, *OCyREF* forced low when $CTR = CCRy$
- 011 - Toggle mode, *OCyREF* toggled when $CTR = CCRy$
- 100 - Force inactive mode, *OCyREF* always forced low
- 101 - Force active mode, *OCyREF* always forced high
- 110 - PWM Mode 1
- 111 - PWM Mode 2

Because the reference signal mode is supposed to be changed during simulation, the OCyM fields can be accessed via the input terminals. Note that those are also updated with the update events generated by the timer.

The hardware options to externally clear the reference signal are not supported in the model. Further, the break function of the timer is not part of the model assuming the flag *BDTR.MOE* is always set. Therefore it is mandatory to set *MOE* to 1 while using the resister-based version.

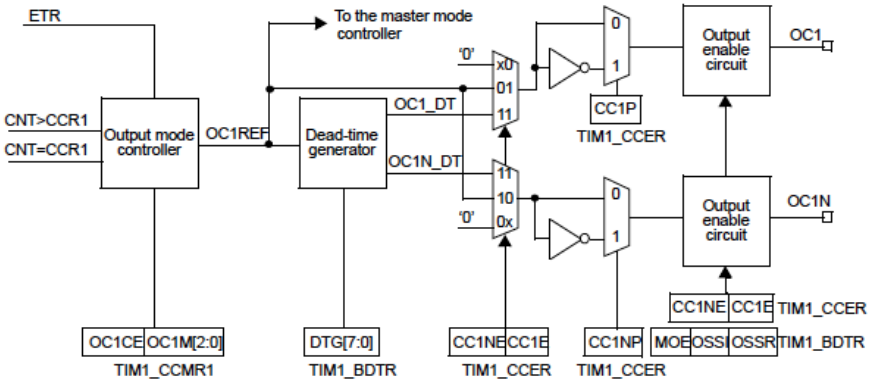
The options available in the output stage majorly depend on the timer subtype and therefore are discussed in the subsequent sections. The configuration of all output stages is done with the *CCER* register.

Note The *CCER* is accessed via the input terminals and is not preloaded. This means that a change on the *CCER* input directly effects the outputs.

---

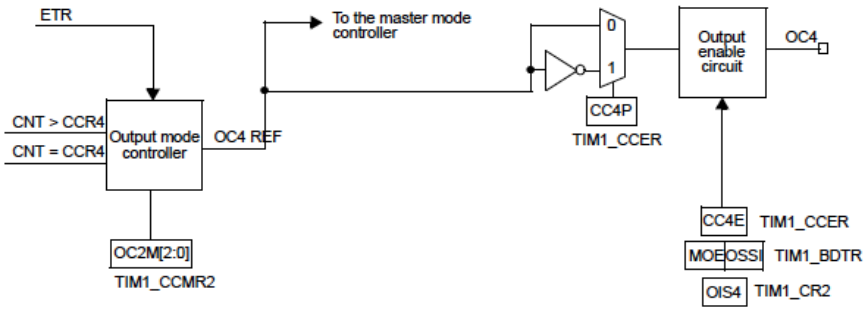
4 Channel Advanced Timer

The Advanced Timer consists of a timer and a 4 channel output stage. The timer has a width of 16-bit and can be operated in Edge-aligned (up and down) as well as Center-aligned mode. For channels 1 to 3, the output stage enables complementary outputs with dead time and configurable polarity.



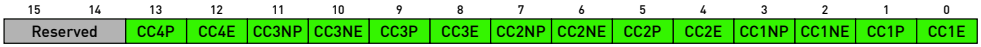
Output stage of Advanced Timer (channel 1 to 3) [1]

For channel 4, the output stage shown below only supports configurable polarity.



Output stage of Advanced Timer (channel 4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.



Channel-wise configuration of output stage

With the CCxP and CCxNP fields, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Those bits further effect the output stage behavior for channels 1 to 3. The table below shows this for both outputs operated with equal polarity.

CCxNE	CCxE	Behavior
0	0	OCx & OCxN inactive
0	1	OCx = OCxREF, OCxN inactive
1	0	OCx inactive, OCxN = OCxREF
1	1	Complementary output mode with dead time

The dead time for each positive flank in *OCx* and *OCxN* is configured with the *TIM_BDTR* register.

Dead time configuration

The dead time (DT) can be calculated based on the cell *DTG* as shown below. The bits *DTG[7:5]* determine the formula used for its calculation.

- $0xx$ - $DT = DTG[7:0] \cdot t_{dtg}$ with $t_{dtg} = t_{DTS}$
- $10x$ - $DT = (64 + DTG[5:0]) \cdot t_{dtg}$ with $t_{dtg} = 2 \cdot t_{DTS}$
- 110 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 8 \cdot t_{DTS}$
- 111 - $DT = (32 + DTG[4:0]) \cdot t_{dtg}$ with $t_{dtg} = 16 \cdot t_{DTS}$

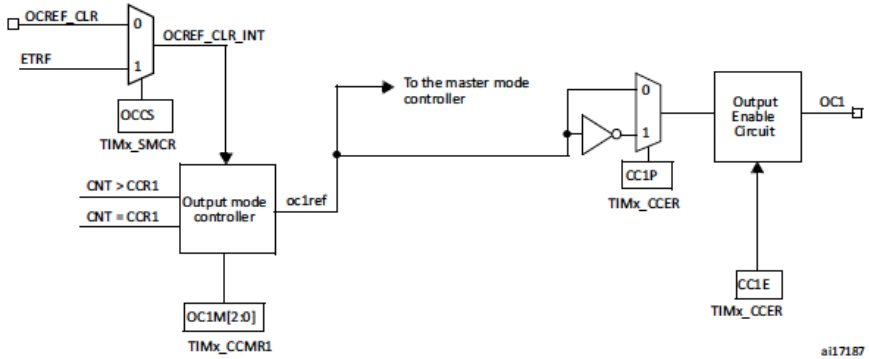
The dead time clock t_{DTS} is related to the timer clock period T_{CK_CNT} and can be configured with the field *CKD* of the *TIM_CR1* register.

- 00 - $t_{DTS} = T_{CK\_CNT}$
- 01 - $t_{DTS} = 2 \cdot T_{CK\_CNT}$
- 10 - $t_{DTS} = 4 \cdot T_{CK\_CNT}$
- 11 - not supported

This subtype implementation uses the full set of inputs, outputs and configuration registers.

4 Channel General Purpose Timer

This subtype is available with a 16-bit or 32-bit counter implementation both supporting Edge-aligned (up and down), as well as Center-aligned modes. The 4 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/4) [1]

The *CCER* register can be used to configure all channels of the output stage separately.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC4NP	Res.	CC4P	CC4E	CC3NP	Res.	CC3P	CC3E	CC2NP	Res.	CC2P	CC2E	CC1NP	Res.	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)

- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CCxNP bits have no effect on the model.

The terminals used by this subtype are shown in the table below.

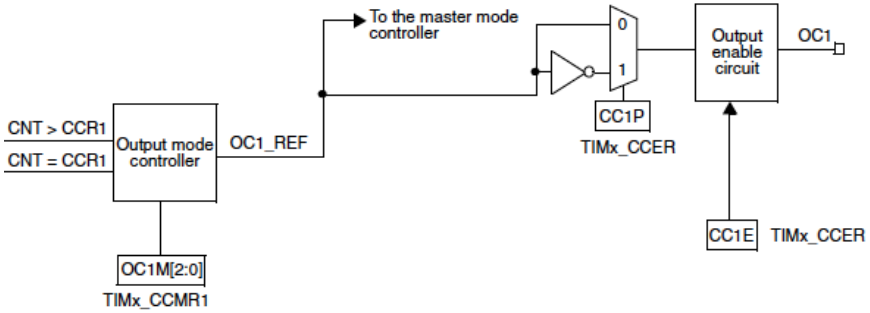
Terminal Group	Utilized	Unused
Input	CCR1 - CCR4, ARR, SYNC, OC1M - OC4M, CCER	x
Output	OC1 - OC4, CC1IF-CC4IF, UIF	OC1N - OC3N

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- GPIO Mode for unused outputs

2 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The 2 channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/2) [1]

The *CCER* register can be used to configure both channels of the output stage separately.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								CC2NP	Res.	CC2P	CC2E	CC1NP	Res.	CC1P	CC1E

Channel-wise configuration of output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CCxNP bits have no effect on the model.

The terminals used by this subtype are shown in the table below.

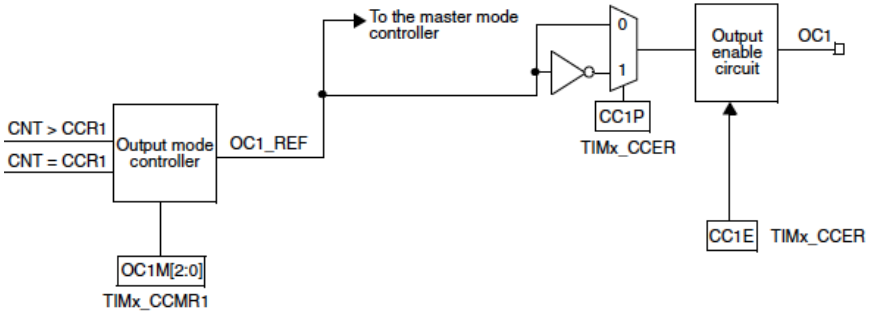
Terminal Group	Utilized	Unused
Input	CCR1 - CCR2, ARR, SYNC, OC1M - OC2M, CCER	CCR3 - CCR4, OC3M-OC4M
Output	OC1 - OC2, CC1IF - CC2IF, UIF	OC3 - OC4, OC1N - OC3N, CC3IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- TIM_DIER.CC3IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

1 Channel General Purpose Timer

This subtype contains a 16-bit counter only supporting Edge-aligned, Upcounting mode. The single channel output stage shown below only supports configurable polarity.



Output stage of general purpose timer (channel 1/1) [1]

The *CCER* register can be used to configure the single channel output stage.

Configuration of the output stage

With the CCxP bits, the polarity of the output signal can be inverted.

- 0 - Active High (regular polarity)
- 1 - Active Low (inverted polarity)

With the CCxE and CCxNE bits, the output can be enabled.

- 0 - Output Enabled, OCx/OCxN defined by OCxREF
- 1 - Output Disabled, OCx/OCxN defined by GPIO Mode

Note The CC1NP bit has no effect on the model.

The terminals used by this subtype are shown in the table below.

Terminal Group	Utilized	Unused
Input	CCR1, ARR, SYNC, OC1M, CCER	CCR2 - CCR4, OC2M-OC4M
Output	OC1, CC1IF, UIF	OC2 - OC4, OC1N - OC3N, CC2IF - CC4IF

Unused mask registers, register cells and further limitations are listed below.

- TIM_BDTR
- TIM_CR1.CKD
- TIM_DIER.CC2IE - TIM_DIER.CC4IE
- GPIO Mode for unused outputs
- TIM_CR1.CMS only supports 00
- TIM_CR1.DIR only supports 0

GPIO Mode

In case that an output enable circuit is configured as inactive, the output level is determined by the GPIO Mode. To mimic this in the simulation model, the parameter GPIO Mode is available in the register-based version.

Configuration of GPIO Mode

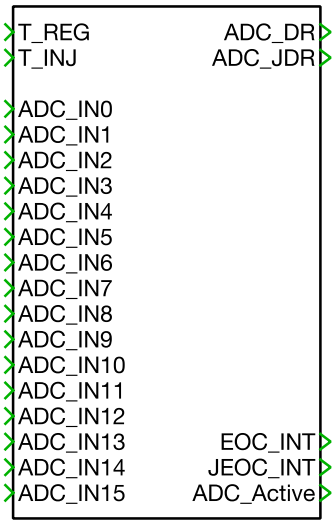
With the bits *OCx* and *OCxN*, the corresponding output mode can be set.

- 0 - Pull-Down (Inactive Low)
- 1 - Pull-Up (Inactive High)

Note This Register is available only in the simulation.

Analog-Digital Converter (ADC)

The PLECS peripheral library provides two blocks for the STM32 F2/F4 single ADC module, one with a register-based configuration mask and a second with a GUI. The figure below shows the appearance of the block.



ADC module model

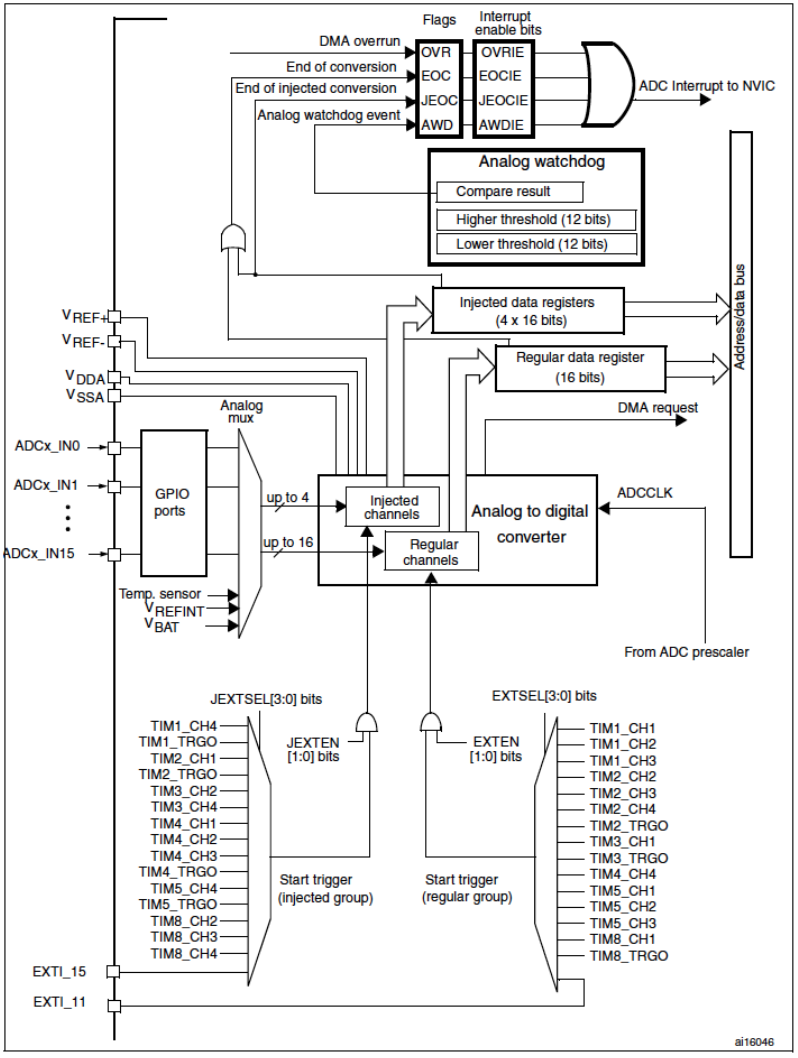
The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a GUI to simplify the configuration.

Both ADC blocks interface with other PLECS components over the following terminal groups.

- *T_REG, T_INJ* - input ports to trigger ADC conversions
- *ADC_INx* - input measurement channels
- *ADC_DR* - auto-size output port to access regular conversion results
- *ADC_JDR* - auto-size output port to access injected conversion results
- *xEOC_INT* - output ports for subsequent logic triggered by a conversion end
- *ADC_Active* - output port indicating an active conversion

ADC Module Overview

The PLECS single ADC model contains the most relevant features of the MCU peripheral.



Overview of the STM F4 ADC module [1]

The ADC model implements these logical submodules:

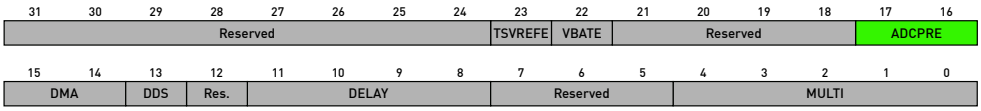
- ADC Converter with Result Registers for Injected and Regular conversion
- ADC Sample Logic for Single, Scan and Discontinuous mode
- ADC Interrupt Logic

For simplicity, the external trigger configuration shown in the figure above is neglected. The trigger to the regular and injected channels are directly accessed via the corresponding input terminals. Further, the Analog Watchdog functionalities as well as the Watchdog and DMA overrun interrupts are not part of the model. Due to simulation efficiency reasons, the ADC can not be operated in continuous conversion mode.

ADC Converter with Result Registers

The ADC module contains a converter with configurable resolution. An external voltage reference is used which can be defined in the component mask.

The period of the ADC clock, and therefore the time base for the module, is determined based on *PCLK2* and the clock divider specified in the *ADC_CCR* register.



ADC_CCER Register structure

By using the *ADCPRE* bits the ADC time base can be specified as follows:

ADCPRE[1]	ADCPRE[0]	ADC clock
0	0	PCLK2 / 2
0	1	PCLK2 / 4
1	0	PCLK2 / 8
1	1	PCLK2 / 16

The resolution of the converter can be specified with the fields *RES* of the *ADC_CR1* register given in the next section. This also influences the amount of ADC clock cycles needed for a conversion. With the *RES* bits the resolution can be specified as shown in the table below.

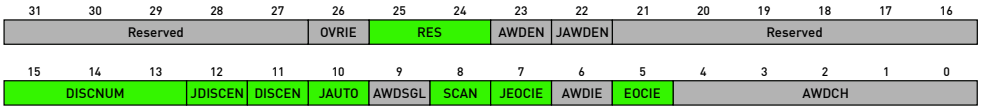
RES[1]	RES[0]	Resolution	Conversion length
0	0	12 bit	15 ADCCLK cycles
0	1	10 bit	13 ADCCLK cycles
1	0	8 bit	11 ADCCLK cycles
1	1	6 bit	9 ADCCLK cycles

For the regular channels, the hardware ADC contains a single 16-bit result register *ADC_DR*. The results of multiple, sequential regular group conversions are typically moved to the *SRAM* on the fly via the *DMA controller*. To simplify this, the *ADC_DR* terminal can provide the conversion result for each of the 16 regular group members separately. For the injected channels, the *ADC_JDR* terminal can provide access to the contents of all four *ADC_JDRx* registers. In the model, both result ports are auto-sized. This means that their width is determined by the length of the regular or injected sequence.

The component only supports the right aligned result representation mode meaning that *ADC_CR2.ALIGN* always needs to be set to 0. In addition to this, the model provides an option to represent the conversion results as quantized double integers, which can be chosen with the mask parameter **Output Mode**.

ADC Sample Logic

The ADC model supports the single, scan and discontinuous conversion modes as well as auto-injected conversions. The continuous conversion mode is not supported due to simulation efficiency reasons. The *ADC_CR1* and *ADC_CR2* registers can be used to choose and control the used conversion mode.



ADC_CR1 Register structure

The *DISCNUM* field defines the number of regular channels converted after a trigger to the regular group was received in discontinuous mode.

DISCNUM	Channels converted
000	1 channel
001	2 channels
...	...
110	7 channels
111	8 channels

The bit *JDISCEN* determines the discontinuous mode for injected channels:

- 0 - Discontinuous mode on injected channels disabled
- 1 - Discontinuous mode on injected channels enabled

With *DISCEN*, the discontinuous mode can be enabled for regular channels:

- 0 - Discontinuous mode on regular channels disabled
- 1 - Discontinuous mode on regular channels enabled

The bit *JAUTO* can be used to automatically trigger an injected group conversion after the regular group was finished:

- 0 - Automatic injected group conversion disabled
- 1 - Automatic injected group conversion enabled

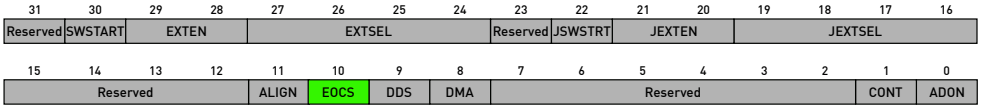
Note Be aware that *JDISCEN* and *DISCEN* exclude each other and *JAUTO* can not be used with discontinuous mode or triggers to the injected group.

With the bit *SCAN*, the user can activate the scan mode of the component allowing multiple conversions triggered by a single event.

- 0 - Scan mode disabled
- 1 - Scan mode enabled

If none of the bits *JDISCEN*,*DISCEN* and *SCAN* is set, the adc module operates in single conversion mode. The bits *JEOCIE* and *EOCIE* are further described in the interrupt section.

For more information about the different conversion modes please refer to [1].



ADC_CR2 Register structure

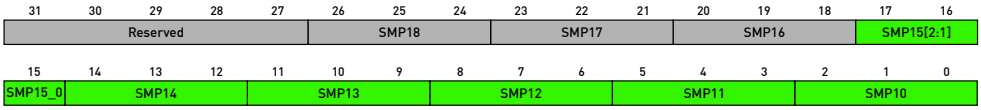
The field *EOCS* configures when the EOC flag is set while not in single conversion mode.

- 0 - EOC is set at the end of each regular group
- 1 - EOC is set at the end of each single regular conversion

---

Note The adc model assumes the adc not to operate in continuous conversion mode and to be always active. Therefore *ADC_CR2.CONT* needs to be cleared and *ADC_CR2.ADON* needs to be set while using the register-based configuration.

For every analog input, the sample time of a conversion can be configured separately using the ADC SMPRx registers.

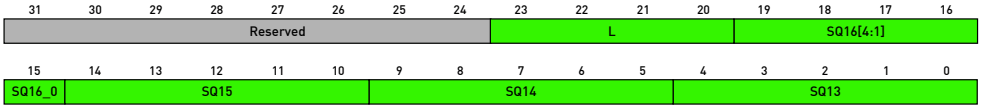


ADC_SMPRx Register structure

Note that *SMP16-SMP18* have no effect because the measurements for the temperature sensor as well as the internal reference and the battery voltage are not part of the model. For every other channel, the sampling time can be configured as follows:

SMPx	Sampling Time
000	3 cycles
001	15 cycles
010	28 cycles
011	56 cycles
100	84 cycles
101	112 cycles
110	144 cycles
111	480 cycles

The ADC operates as a sequencer which has a maximum sequence of 16 conversions for the regular group and 4 conversions for the injected group. The input sampled by each group element as well as the sequence length can be configured via the *ADC_SQRx* and the *ADC_JSQR* registers.



ADC_SQRx Register structure

The length of the regular sequence is defined by the field *L*.

L	Sequence length	Converted elements / ADC_DR
0000	1 conversion	[SQ1]
0001	2 conversion	[SQ1 SQ2]
...	...	...
1111	16 conversions	[SQ1 SQ2 ... SQ16]

ADC_JSQR Register structure

The length of the injected sequence is defined by the field *JL*.

JL	Sequence length	Converted elements / ADC_JDR
00	1 conversion	[JSQ4]
01	2 conversion	[JSQ3 JSQ4]
...	...	...
11	4 conversions	[JSQ1 JSQ2 JSQ3 JSQ4]

After the last conversion is finished, the sequencer wraps around and restarts with the first element after the next trigger was received.

For every sequence element, the sampled input can be specified via the corresponding *SQx* or *JSQx* fields as follows:

SQx/JSQx	Input
x0000	ADC_IN0
x0001	ADC_IN1
...	...
x1111	ADC_IN15

Note The terminals *ADC_DR* and *ADC_JDR* are auto-size output terminals. This means that the width of the terminals is defined by *J* or *JL* as shown in the upper tables.

ADC Interrupt Logic

The ADC module also has a connection to the *NVIC* of the *STM F2/F4 MCU*. The *EOC* flag is set when either the regular channel or the injected channel indicates an end of conversion. The *JEOC* flag is set when the injected group indicates a finished conversion. The fields *ADC_CR1.EOCIE* and *ADC_CR1.JEOCIE* can be used to configure the adc to provide an interrupt pulse to the corresponding output terminals.

- 0 - no interrupt pulses are generated at the EOC_INT/JEOC_INT terminal
- 1 - interrupt pulses are generated at the EOC_INT/JEOC_INT terminal

Even if there typically won't be a model of the *NVIC* within the simulation, those pulses can i.e. be used to trigger the PIL block modeling a control step triggered by a finished adc conversion.

Reference

1 - Literature Source: STM32 Reference Manual [RM0090] or [RM0033]

8

Microchip dsPIC33F Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical

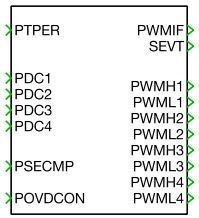
user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

Microchip Motor Control PWM

The PLECS peripheral library provides two blocks for the Microchip Motor Control PWM (MCPWM) module, one with a register-based configuration mask and a second with a graphical user interface. The figure below shows the register-based version of the MCPWM module.



Register-based MCPWM module model

The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a graphical user interface to simplify the configuration.

Both MCPWM blocks interface with other PLECS components over the following terminal groups:

- *PDCx* - input ports for duty cycle register
- *PSECMP* - input port for special event trigger compare register
- *POVDCON* - input port for override control register
- *PWMIF* - output port for PWM interrupt flag
- *SEVT* - output port for special event trigger
- *PWMHx/Lx* - output ports for PWM signals

Note In the PLECS MCPWM module, PWM Faults have not been modeled

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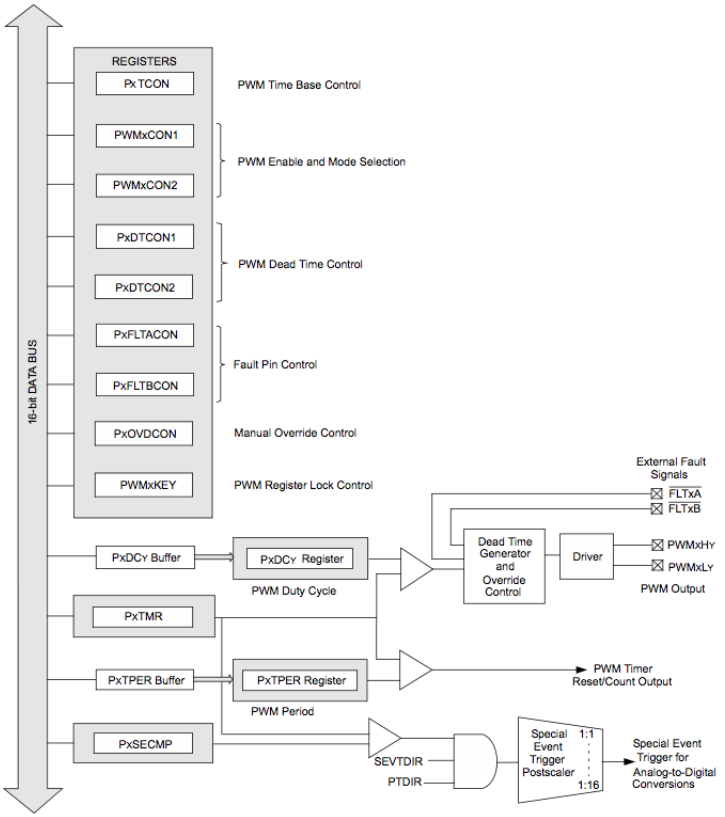
MCPWM Module Overview

The PLECS MCPWM model implements the most relevant features of the MCU peripheral.



Overview of the MCPWM module[1]

The MCPWM model implements the following features:

- PWM Clock Control
- PWM Output Control and Resolution
- PWM Output Override
- Interrupt Control
- Special Event Trigger

- Dead Time Generator

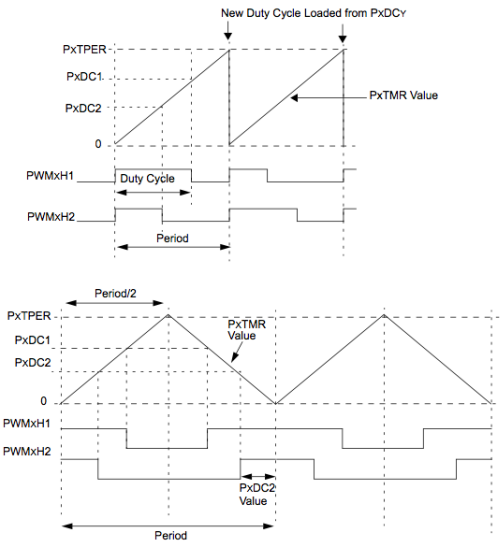
A section summarizing the differences of the PLECS MCPWM module as compared to the actual MCPWM module is provided in the “Summary” (on page 263) section.

PWM Clock Control

The modeled MCPWM realizes a counter that can operate in three different modes for the generation of asymmetrical and symmetrical PWM signals. The three supported modes are:

- *Free Running mode*
- *Continuous Up/Down mode*
- *Continuous Up/Down mode with interrupts for double PWM updates*

The counter for these modes is visualized below.



Counter modes [1]

In *Free Running mode*, the counter is incremented from 0 to a counter period *PTPER* using a counter clock operated at a clock frequency of F_{CY}. The *PTPER* value corresponding to a desired PWM frequency (F_{PWM}) can be calculated as:

$$PTPER = \frac{F_{CY}}{F_{PWM} \cdot PTMR\ Prescaler} - 1$$

When the counter reaches the period (*PTPER*), the subsequent count value is reset to zero, duty cycle (*PDCx*) and special event (*PSECMP*) registers are updated, and the sequence is repeated.

In the *Continuous Up/Down mode*, and *Continuous Up/Down mode with interrupts for double PWM updates*, the counter is incremented from 0 to a counter period *PTPER* and then decremented back to 0 using a counter clock operated at a clock frequency of F_{CY}. The *PTPER* value corresponding to a desired PWM frequency (F_{PWM}) can be calculated as:

$$PTPER = \frac{F_{CY}}{2 \cdot F_{PWM} \cdot PTMR\ Prescaler} - 1$$

In the *Continuous Up/Down mode*, when the counter reaches 0, the duty cycle (*PDCx*) and special event (*PSECMP*) registers are updated.

In the *Continuous Up/Down mode with interrupts for double PWM updates*, the duty cycle (*PDCx*) and special event (*PSECMP*) registers are updated when the counter reaches 0 and *PTPER*.

Note In the PLECS MCPWM module, *Single Event Mode* is not allowed.

While the system clock and the period counter value are separately defined in the mask parameters, the counter mode and the clock divider are jointly configured in the *PTCON* register.

PTCON Register Configuration [1]

The input clock (T_{CY}) derived from the oscillator source can be prescaled using the *PTCKPS* bits in the *PTCON* register. Additionally, the counter mode selected using the *PTMOD* bits and the time-based output post scalar (*PTOPS*) bits determine the generation of the PWM interrupt flag.

Example Configuration – Step 1

This example shows the configuration of the PWM module operating in *Free Running mode* with a 50 μs period. The *PTCON* register is configured to:

$$PTCON = 4 \;\hat{=}\; 0\,0\,0\,0\,0\,0\,0\,0\,\underbrace{0\,0\,0\,0}_{PTOPS}\;\underbrace{0\,1}_{PTCKPS}\;\underbrace{0\,0}_{PTMOD}$$

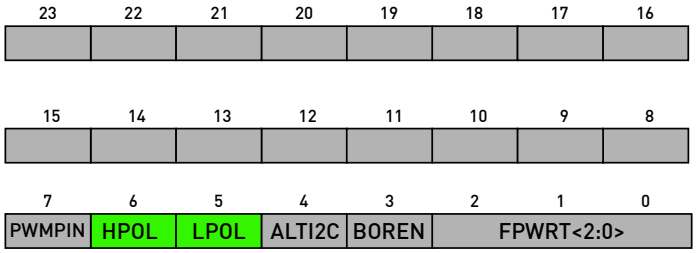
According to this configuration, the time-based submodule is operating in the *Free Running mode* with a timer clock period four times the system clock period. For a *PTPER* value of 999 and an 80 MHz system clock, the resulting PWM signal has the following period:

$$T_{PWM} = (PTPER + 1) \cdot \frac{PTCKPS}{F_{CY}} = 50\ \mu s.$$

PWM Output Control and Resolution

The MCPWM model for a non-zero duty cycle results in outputs of the PWM generators to be driven active at the beginning of the PWM period. Each PWM output will be driven inactive when the value of the counter matches the duty cycle value of the PWM generator. If the value of the duty cycle register is zero, the output on the corresponding PWM pin is inactive for the entire PWM period. The PWM output is active for the entire period if the value of *PDC* is greater than *PTPER*.

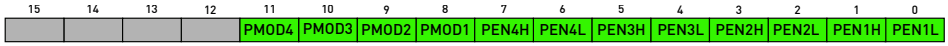
Note In the implemented model, immediate update of the *PDC* and *PSECMP* registers is not modeled.



FPOR:POR Register Configuration [1]

The *HPOL* and *LPOL* bits in the *FPOR:POR* register determine the output polarity of the high-side and low-side output pins of the PWM generators. For example, if the *LPOL* bit is set, then the low-side output is high when the PWM is active and low when the PWM is inactive. If the bit is cleared, then

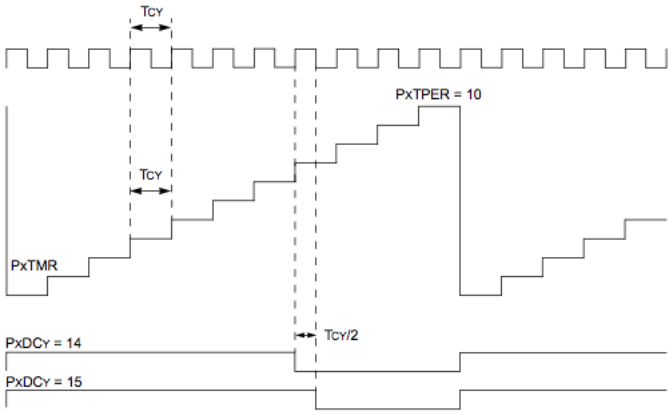
the low-side output is low when the PWM is active and high when the PWM is inactive.



PWMCON1 Register Configuration [1]

In the MCPWM, each PWM generator can be operated in either complementary or independent mode. In complementary mode both output pins cannot be active simultaneously. Additionally, a dead time is inserted during device switching making both outputs inactive for a short period. In independent mode there are no restrictions on the state of the pins for a given output pin pair. Additionally, the dead time module is disabled when the PWM module is operated in independent mode. The mode for each of the PWM generators is selected by configuring the bits *PMOD4:PMOD1* in the *PWMCON1* register.

The first bit of the register *PDC* determines whether the PWM signal edge occurs at the T_{CY} or $\frac{T_{CY}}{2}$ boundary. The figure below illustrates the effect of this bit on the PWM output.

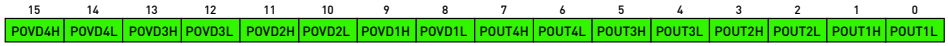


Duty cycle resolution timing diagram, Free Running mode, and 1:1 prescaler selection [1]

PWM Output Override

The output pins of the MCPWM module can be configured to be manually driven to a specific state, independent of the duty cycle comparison units. This

feature is useful when controlling various types of electrically commuted motors. The *POVDCON* register is used to control the override function for each PWM output.



POVDCON Register Configuration [1]

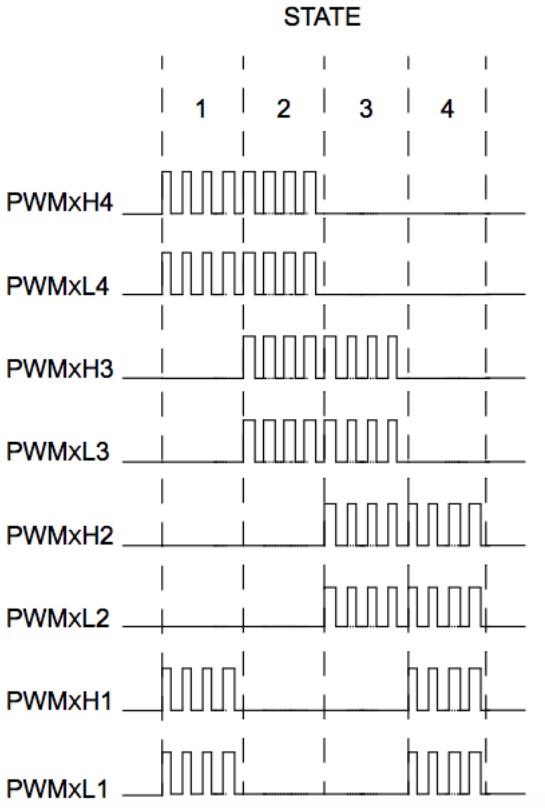
The *POVDxL*/*H* bits in the *POVDCON* register are used to control whether the corresponding PWM pins will be overridden. The *POUTxL*/*H* bits in the *POVDCON* register are used to control the state of the corresponding PWM output pins. When the *POVDxH*/*L* bits are set, the corresponding PWM outputs are controlled by the corresponding duty cycle comparison unit. When the *POVDxH*/*L* bits are cleared, the corresponding PWM outputs are controlled by state of the corresponding *POUTxL*/*H* bits. If the *POUTxL*/*H* bit is set then the PWM output is driven to an active state. When the *POUTxL*/*H* bit is cleared, the PWM output is driven to an inactive state.

When operated in *Complementary PWM Output Mode*, the MCPWM does not allow a pair of PWM pins to become simultaneously active thus restricting some override configurations. In complementary output mode, the high-side pin takes priority. Also, in this mode the dead time insertion is still performed even when PWM channels are overridden manually.

If the output synchronization bit (*OSYNC*) is set, all output override performed using the *POVDCON* register will be synchronized to the PWM time base. The synchronization for both center-aligned and edge aligned mode occurs when the counter is at zero. This functionality allows the generation of an unwanted narrow pulse on the PWM output pins.

Note When *OSYNC* bit is cleared, the PLECS MCPWM module assumes that the *POUT* input signals are synchronized to the T_{CY} clock. Thus the corresponding PWM pins are set or cleared instantaneously.

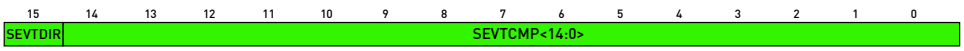
The override bits can be used to control commutation of the PWM outputs. In this example, all the PWM pairs in the MCPWM module are operated in independent mode. The duty cycle compare unit can be used in conjunction with the *POVDCON* register. This enables the user to control the current delivered to the load using the duty cycle compare unit and the *POVDCON* register to control the commutation.



PWM output override example [1]

Special Event Trigger

The MCPWM can be configured to trigger the Analog-to-Digital (ADC) converter using the special event compare register (*PSECMP*). This allows ADC sampling and conversion timing to be synchronized to the PWM time base and provides the flexibility of programming the start of conversion at any point within the PWM period.



PSECMP Register Configuration [1]

The PWM counter register is compared to the *SEVTCMP* bits in the *PSECMP* register and generates a trigger signal when the counter value is equal to the *SEVTCMP* bits. In *Up/Down Count mode*, the *SEVTDIR* bit provides added flexibility on the generation of the trigger signal. When this bit is set, the trigger is generated on a match event when the counter is counting down. When the bit is set to zero, the trigger is generated on a match event when the counter is counting up.

Additionally, the Special Event Trigger Postscaler (*SEVOPS*) bits in the *PWMCON2* register allows a 1:1 to 1:16 post scale ratio. These bits can be configured if the ADC conversions are not required every PWM cycle.

PWMCON2 Register Configuration [1]

Interrupt Control

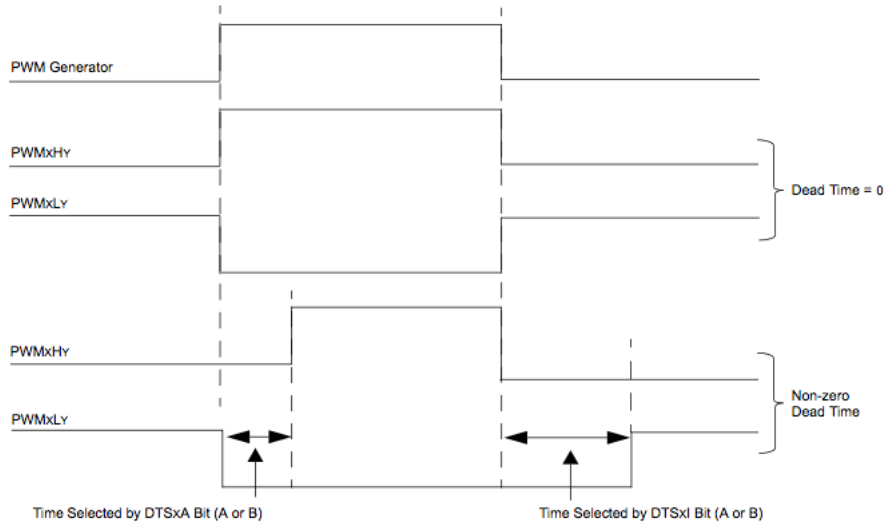
The MCPWM module can be configured to generate an interrupt flag depending on the mode of operation and the time base postscaler (*PTOPS*) bits in the *PTCON* register. In the model the interrupt flag (*PWMIF*) is internally reset automatically after one simulation step.

In the *Continuous Up/Down mode with interrupts for double PWM updates*, an interrupt event is generated each time the counter equals 0 and *PTPER*. The postscaler selection bits are ignored in this mode.

In the *Free Running mode* the interrupt flag is generated when the counter is reset to 0. In the *Continuous Up/Down mode*, the interrupt flag is generated when the counter is equal to 0 and the counter is counting up. In both of these modes, the postscaler bits can be used to reduce the frequency of interrupt events.

Dead Time Generator

In independent mode, the dead-time module is inactive and no dead-time is inserted between the high-side and low-side PWM signals of a PWM output generator. When operated in complementary mode, each PWM output generator can be configured to have some dead time between the turn on and turn off of the high-side and low-side PWM signals.



Dead time insertion [1]

The Dead Time Control Register 1 (*PDCTON1*) is used to configure two different dead-time units (Unit A and Unit B). The *DTA* bits are used to assign a 6-bit dead-time value for Unit A. The *DTAPS* bit is used to configure the dead-time clock as a multiple of the system clock (T_{CY}). The corresponding bits *DTB* and *DTBPS* are used to configure Unit B.

PDTCON1 Register Configuration [1]

The dead-time for Unit A and Unit B, are calculated as follows:

$$Dead\ Time = (DTx + 1) \cdot T_{CY} \cdot DTxPS,$$

where x refers to Unit A or B.

The Dead Time Control Register 2 (*PDCTON2*) contains configuration bits that are used to control the insertion of dead time when the high-side or low-side PWM signals become active. The *DTS1I* - *DTS4I* bits select the dead time inserted before *PWML1* - *PWML4*, respectively, are driven active. The *DTS1A* - *DTS4A* bits select the dead time inserted before *PWMH1* - *PWMH4*, respectively, are driven active.

PDTCON2 Register Configuration [1]

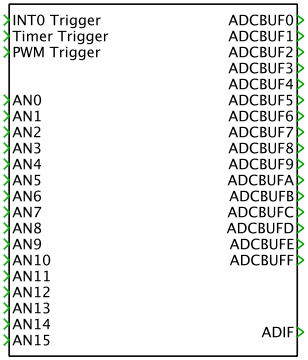
Summary of PLECS Implementation

The PLECS MCPWM module models the major functionality of the actual MCPWM module. Below is a summary of differences of the PLECS MCPWM module compared to the actual MCPWM module:

- PWM Faults are not supported.
- *Single Event Mode* is not supported.
- Immediate update of the *PDC* and *PSECMP* registers is not supported.
- When *OSYNC* bit is cleared, the PLECS MCPWM module assumes that the *POUT* input signals are synchronized to the T_{cy} clock. Thus the corresponding PWM pins are set or cleared instantaneously.
- PWM update lockout is not supported.
- The interrupt flag (*PWMIF*) is internally reset automatically after one simulation step.

Microchip Motor Control ADC

The PLECS peripheral library provides two blocks for the Microchip Motor Control ADC (MCADC) module, one with a register-based configuration mask and a second with a graphical user interface. The figure below shows the appearance of the register-based version.



Register-based MCADC module model

The register-based version allows the user to directly enter register values in decimal, binary, or hexadecimal notation. For convenience, the peripheral library also provides a component with a graphical user interface to simplify the configuration.

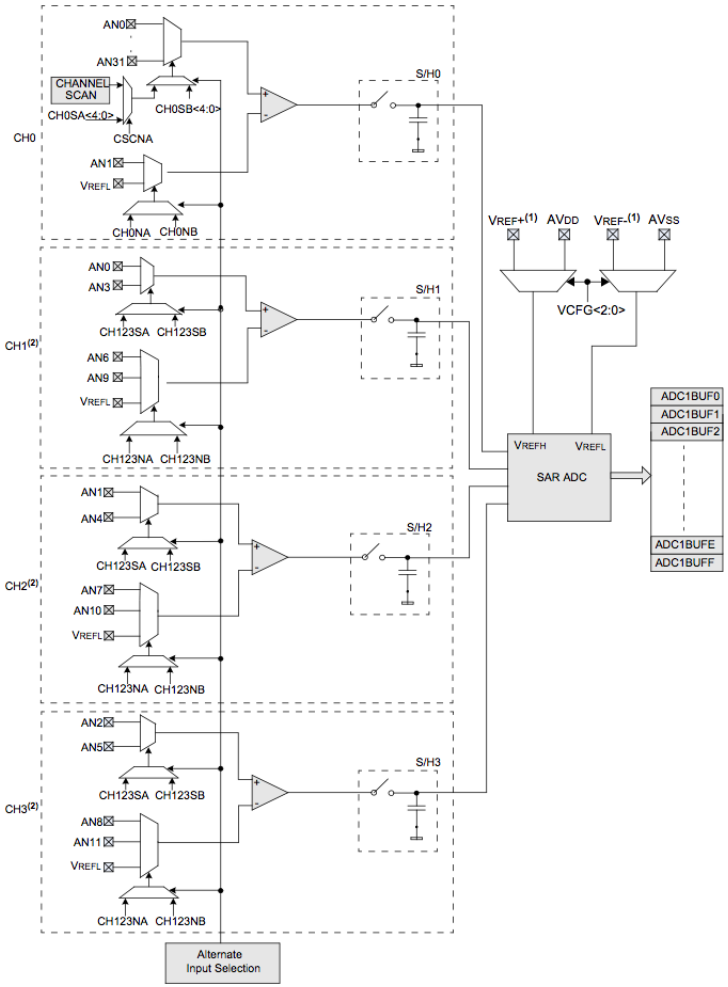
Both MCADC blocks interface with other PLECS components over the following terminal groups:

- *ANx* - input ports for duty cycle register
- *Triggers* - input port for INT0, Timer, and PWM triggers
- *ADCBUFx* - output port for ADC buffer register
- *ADIF* - output port for ADC interrupt flag

Note In the PLECS MCADC module, the GP timer triggers (Timer 3 and Timer 5) and Motor Control PWM 1 and 2 triggers have been lumped into a single Timer and PWM trigger, respectively.

MCADC Module Overview

The PLECS MCADC model implements the most relevant features of the MCU peripheral.



Overview of the MCADC module without DMA [2]

The MCADC model implements the following features:

- ADC Configuration

- ADC Sampling and Conversion
- Multi-channel ADC Sampling Mode
- ADC Input Selection Mode
- ADC Interrupt Logic
- ADC Buffer Fill Mode

A section summarizing the limitation of the PLECS MCADC module as compared to the actual MCADC module is provided in the “Summary” (on page 274) section.

ADC Configuration

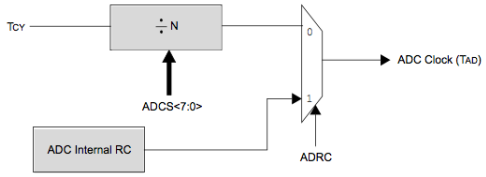
The MCADC module can be operated either in 10-bit or 12-bit operation mode. The 12-bit Operation Mode bit (*AD12B*) in the *ADCON1* register allows the ADC module to function as either a 10-bit, 4-channel ADC (when the *AD12B* bit is cleared) or a 12-bit, single-channel ADC (when the *AD12B* bit is set). In 10-bit mode, the *CHPS* bits in the *ADCON2* register can be configured to operate the MCADC module to convert:

- only $CH0$
- $CH0$ and $CH1$
- $CH0$, $CH1$, $CH2$, and $CH3$

The *VCFG* bits in the *ADCON2* register allow the selection of the voltage references for the MCADC module. The voltage reference high (V_{REFH}) and the voltage reference low (V_{REFL}) for the ADC module can be supplied from the internal AV_{DD} and AV_{SS} voltage rails or the external V_{REF+} and V_{REF-} input pins. The table below summarizes the different configurations that are possible by setting the *VCFG* bits.

VCFG	V_{REFH}	V_{REFL}
000	AV_{DD}	AV_{SS}
001	AV_{DD}	V_{REF-}
010	V_{REF+}	AV_{SS}
011	V_{REF+}	V_{REF-}
1xx	AV_{DD}	AV_{SS}

The MCADC module clock (T_{AD}) can be configured to use the system clock (T_{CY}) or a dedicated internal RC clock (T_{ADRC}). The figure below summarizes the generation of the ADC clock.



ADC Clock Generation [2]

While the system clock and the period counter value are separately defined in the mask parameters, the ADC clock source selection (*ADRC*) and the clock divider (*ADCS*) are jointly configured in the *ADCON3* register.

ADCON3 Register Configuration [2]

The clock divider is used to lower the frequency when the ADC clock is derived from the system clock. The *ADCS* bits allow the clock to be scaled to one of 64 settings, from 1:1 to 1:64. The table below summarizes the effect the *ADCS* and *ADRC* bits have on the ADC clock period.

ADRC	ADC Clock Period (T_{AD})
0	$T_{CY} \cdot (\text{ADCS} + 1)$
1	T_{ADRC}

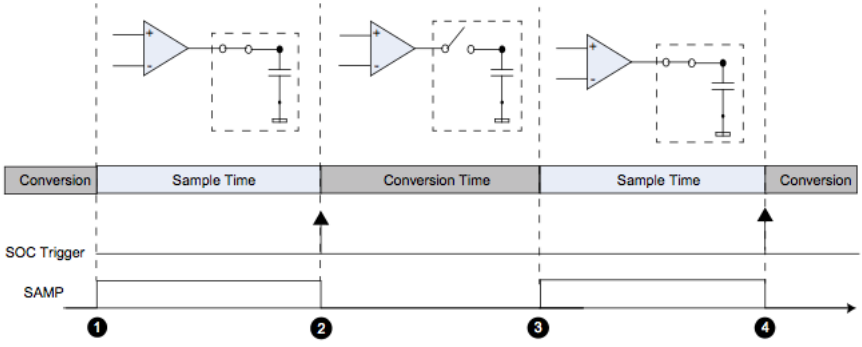
Note *ADCS* values over 63 are reserved in the actual hardware and will be flagged as an error in the PLECS MCADC module.

The MCADC module can be configured to output the ADC results in four different numerical formats. The *FORM* bits in the *ADCON1* register select the data format. Further, in the PLECS MCADC module the output format can be configured as quantized double format for convenience. The Output mode

block parameter selects if the *FORM* bits are used or if the output is presented as a quantized double format. The table below summarizes the different available formats.

FORM	Output Mode	Data Format
00	Use FORM bits	Unsigned Integer
01	Use FORM bits	Signed Integer
10	Use FORM bits	Unsigned Fractional
11	Use FORM bits	Signed Fractional
xx	Quantized Double	Quantized Double

ADC Sampling and Conversion



Note 1: Sampling starts automatically after conversion.
2: Conversion starts upon trigger event.
3: Sampling starts automatically after conversion.
4: Conversion starts upon trigger event.

Automatic Sample and Triggered Conversion Sequence [2]

The actual MCADC module can be configured to operate in different modes. Below is a list of the possible configurations for the actual MCADC:

- Manual Sample and Manual Conversion Sequence
- Manual Sample and Automatic Conversion Sequence
- Manual Sample and Triggered Conversion Sequence

- Automatic Sample and Manual Conversion Sequence
- Automatic Sample and Automatic Conversion Sequence
- Automatic Sample and Triggered Conversion Sequence

In the PLECS MCADC module only the Automatic Sample and Triggered Conversion Sequence mode has been modeled. The figure above summarizes the operation of this mode.

In this mode, the sampling of the channels starts automatically after a conversion is completed. Automatic sampling is enabled by setting the *ASAM* bit in the *ADCON1* register. The conversion is started upon trigger event from one of the external SOC trigger sources. This allows ADC conversion to be synchronized with the internal or external events. The external trigger source is selected by configuring the *SSRC* bits to

- 001 when using External Interrupt Trigger
- 010 or 100 when using Timer Interrupt Trigger
- 011 or 101 when using Motor Control PWM Special Event Trigger

---

Note In the PLECS MCADC module, clearing the *ASAM* bit is not allowed. This bit must always be set. Additionally, in the actual hardware the ADC module takes some time to stabilize. There is no such requirement in the implemented MCADC module.

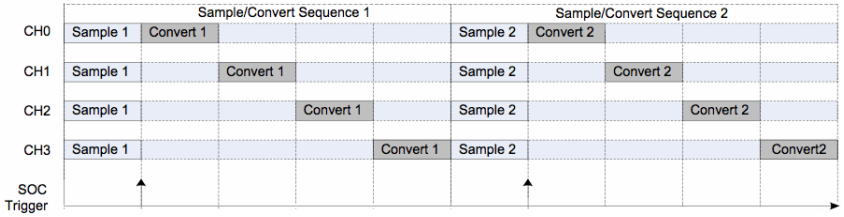
The MCADC can be operated either as a single-channel 12-bit or multi-channel 10-bit module. The time required to complete a conversion (T_{CONV}) is dependent on whether the ADC is operated in 12-bit or 10-bit mode. The table below summarizes the amount of time required to completed one conversion in the two modes:

Mode	T_{CONV}
10-bit	$12 \cdot T_{AD}$
12-bit	$14 \cdot T_{AD}$

Multi-channel ADC Sampling Mode

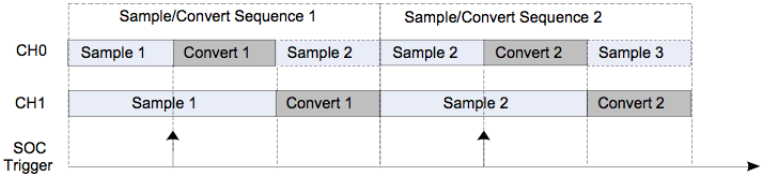
The MCADC works as single channel converter when operated in as a 12-bit ADC module. In this mode the inputs to $CH1$, $CH2$, and $CH3$ are ignored and

only $CH0$ is converted. When operated as a 10-bit ADC module, the MCADC can be configured to operate as a multi-channel ADC module. In the multi-channel operation, the MCADC module can be configured to operate in simultaneous or sequential sampling modes. In simultaneous sampling mode, the sampling of all channels is stopped when an SOC trigger is received. The figure below shows the timing diagram of a 4-channel module operated with simultaneous sampling in the Automatic Sample and Triggered Conversion Sequence mode.



4-Channel Simultaneous Sampling [2]

When the multi-channel ADC module is operated in sequential mode, the sampling for $CH0$ ends when an SOC trigger is received. The sampling of $CH1$ ends once the conversion of $CH0$ is completed. The same logic applies to the end of sampling for $CH2$ and $CH3$. The figure below shows the timing diagram of a 2-channel module operated with sequential sampling in the Automatic Sample and Triggered Conversion Sequence mode.

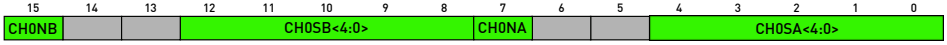


2-Channel Sequential Sampling [2]

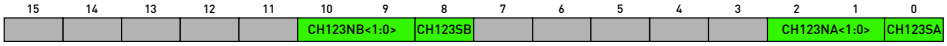
Note Any SOC trigger received while the MCADC module is converting will be lost. Conversions are started when an SOC trigger is received while the module is sampling all active channels.

ADC Input Selection Mode

The *ADCHS0* and *ADCHS123* registers are used to configure which analog input channels are selected as the positive and negative input selections for $CH0$, and $CH1$, $CH2$, and $CH3$, respectively. The figures below show the two registers:



ADCHS0 Register Configuration [2]



ADCHS123 Register Configuration [2]

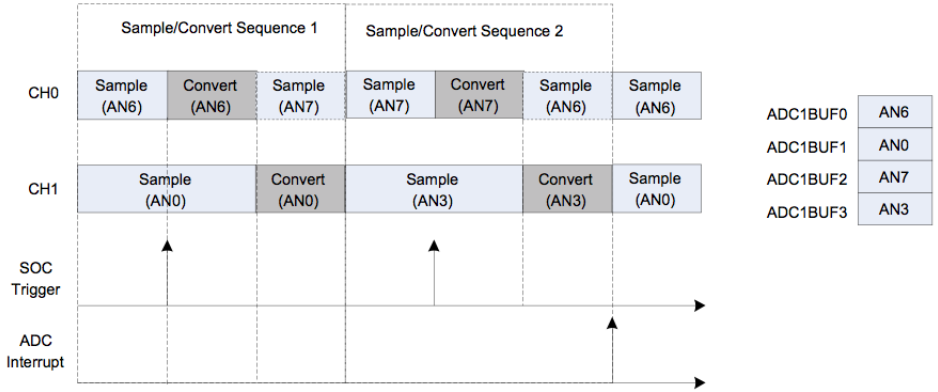
In the MCADC module, each channel can be configured to operate in fixed input selection mode which uses only MUXA, or in alternate input selection mode where both MUXA and MUXB are used. The table below summarizes the effect of the control bits on the analog input selection for each channel.

		MUXA		MUXB	
		Control bits	Analog Inputs	Control bits	Analog Inputs
CH0	+ve	CH0SA<4:0>	AN0 to AN31	CH0SB<4:0>	AN0 to AN31
	-ve	CH0NA	VREF-, AN1	CH0NB	VREF-, AN1
CH1	+ve	CH123SA	AN0, AN3	CH123SB	AN0, AN3
	-ve	CH123NA<1:0>	AN6, AN9, VREF-	CH123NB<1:0>	AN6, AN9, VREF-
CH2	+ve	CH123SA	AN1, AN4	CH123SB	AN1, AN4
	-ve	CH123NA<1:0>	AN7, AN10, VREF-	CH123NB<1:0>	AN7, AN10, VREF-
CH3	+ve	CH123SA	AN2, AN5	CH123SB	AN2, AN5
	-ve	CH123NA<1:0>	AN8, AN11, VREF-	CH123NB<1:0>	AN8, AN11, VREF-

When operated in fixed input selection mode, chosen by setting the *ALTS* bit in the *ADCON2* register to zero, only MUXA and the associated control bits are used to select the positive and negative analog inputs for each channel. When operated as a 12-bit module, only $CH0$ is sampled.

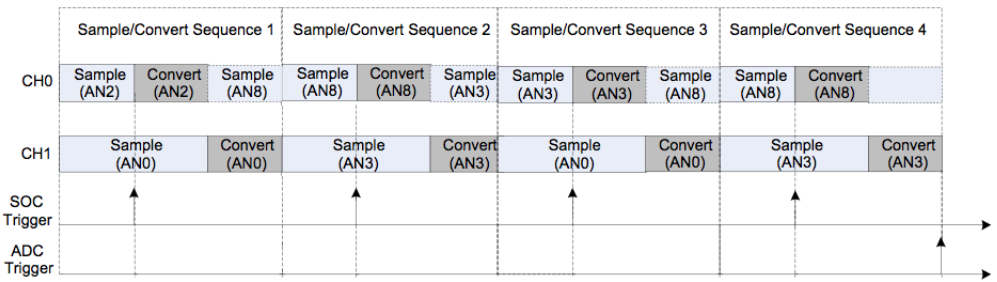
When operated in alternate input selection mode, chosen by setting the *ALTS* bit in the *ADCON2* register to 1, both MUXA and MUXB are used to select the positive and negative analog inputs for each channel. Again, when operated as a 12-bit module, only $CH0$ is sampled. In this mode the ADC completes one sweep using the MUXA selection and uses the MUXB selection in

the next sweep. In the next sweep MUXA is used again. This switch between MUXA and MUXB continues while the ADC is operated in this mode. The figure below shows the operation of a 2-channel module with alternate input selection in sequential sampling mode. The interrupt has been configured to occur after 4 conversions.



2-Channel Sequential Sampling in Alternate Input Selection mode [2]

The MCADC module provides further flexibility by allowing $CH0$ to be operated in scan mode. The Channel Scanning mode is enabled by setting the Channel Scan bit (*CSCNA*) in the *ADCON2* register.



2-Channel Sequential Sampling in Alternate Input Selection mode with Channel Scan enabled [2]

The desired conversion sequence is selected by configuring the appropriate bits in the channel selection register (*AD1CSSL*). The conversions are carried out in ascending order. If operated in alternate input selection mode with channel scan enabled, MUXA software control is ignored for $CH0$ and the

ADC module converts the first selected analog input. In the next sweep, the inputs selected by MUXB are measured. In the following sweep the next selected analog input is sampled for $CH0$. Input selections for $CH1$, $CH2$, and $CH3$ are unaffected. The figure above shows an example of a 2-channel sequential sampling module operated in alternate input selection mode with channel scanning enabled. $AN2$ and $AN3$ have been selected for channel scanning and $AN8$ has been selected by the MUXB input selector for $CH0$. An interrupt is generated after 8 conversions.

ADC Interrupt Logic

CHPS	SIMSAM	SMPI	Conversions per Interrupt	Description
00	x	N-1	N	1-Channel mode
01	0	N-1	N	2-Channel, Sequential Sampling mode
1x	0	N-1	N	4-Channel, Sequential Sampling mode
01	1	N-1	$2 \cdot N$	2-Channel, Simultaneous Sampling mode
1x	1	N-1	$4 \cdot N$	4-Channel, Simultaneous Sampling mode

The PLECS MCADC module reflects the properties of an actual MCADC module without DMA. The ADC module writes the results of the conversions into the analog-to-digital result buffer as conversions are completed. The *SMPI* bits in the *ADCON2* register determine the number of conversions for the MCADC module before an interrupt is generated. The results are written into the ADC buffer after each conversion is completed. The MCADC module supports 16 result buffers. Therefore, the maximum number of conversions per interrupt must not exceed 16.

The number of conversions per ADC interrupt depends on the following parameters, which can vary from one to 16 conversions per interrupt:

- Number channels selected
- Sequential or Simultaneous Sampling
- Samples Convert Sequences Per Interrupt bits (*SMPI*) settings

The table above summarizes the effect each of these factors has on the number of conversions per interrupt.

ADC Buffer Fill Mode

When the Buffer Fill Mode bit (*BUFM*) in the *ADCON2* register is set, the 16-word results buffer is split into two 8-word groups: a lower group (ADC1BUF0 through ADC1BUF7) and an upper group (ADC1BUF8 through ADC1BUFF). The 8-word buffers alternately receive the conversion results after each ADC interrupt event. When the *BUFM* bit is set, each buffer size equals eight. Therefore, the maximum number of conversions per interrupt must not exceed 8. When the *BUFM* bit is cleared, the complete 16-word buffer is used for all conversion sequences.

Summary of PLECS Implementation

The PLECS MCADC module models the major functionality of the actual MCADC module. Below is a summary of differences of the PLECS MCADC module compared to the actual MCADC module:

- The PLECS MCADC module models the Microchip MCADC module without DMA.
- The GP timer triggers (Timer 3 and Timer 5) and the Motor Control PWM 1 and 2 triggers have been lumped together into single Timer and PWM trigger, respectively.
- *ADCS* values over 63 in the *ADCON3* register will be flagged as an error in the PLECS MCADC module.
- Only Automatic Sample and Triggered Conversion Sequence mode is supported by the PLECS MCADC module. Clearing the *ASAM* bit in the *ADCON1* register will be flagged as an error.
- The PLECS MCADC module does not require any time for stabilization during startup.
- Any SOC trigger received while the MCADC module is converting will be lost. Conversions are started when an SOC trigger is received while the module is sampling all active channels.
- The output results are provided according to the numerical format specified by the *FORM* bits in the *ADCON1* register or as quantized double values.

Reference

1 - Pictures provided with Courtesy of Microchip, Literature Source: *Motor Control PWM Reference Guide*, Literature Number DS70187E, February 2007 - Revised September 2012

2 - Pictures provided with Courtesy of Microchip, Literature Source: *Motor Control ADC Reference Guide*, Literature Number DS70183D, December 2006 - Revised April 2012

9

Infineon XMC1xxx Peripheral Models

Introduction

Microcontrollers (MCUs) for control applications typically contain peripheral modules such as Analog-to-Digital Converters (ADCs) and pulse width modulators (PWMs). These peripherals play an important role, since they act as the interface between the digital/analog signals of the control hardware and the control algorithms running on the processor. State-of-the-art MCUs often include peripherals with a multitude of advanced features and configurations to help implement complex sampling and modulation techniques.

When modeling power converters in a circuit simulator such as PLECS, it is desirable to represent the behavior of the MCU peripherals as accurately as possible. Basic Sample&Hold blocks and PWM modulators are useful for higher-level modeling. However, important details with regards to timing and quantization are lost when attempting to model an ADC with a basic zero-order hold (ZOH) block. For example, employing an idealized modulator to generate PWM signals can result in simulation results substantially different from the real hardware behavior.

Accurate peripheral models are even more important in the context of Processor-In-the-Loop (PIL) simulations. In this case, it is imperative to utilize peripheral models which are configurable exactly as the real implementations, i.e. by setting values in peripheral registers. By the same token, the inputs and outputs of the peripheral models must correspond precisely to the numerical representation in the embedded code.

The PLECS PIL library includes high-fidelity MCU peripheral models which work at the register level, and are therefore well-suited for PIL simulations. Furthermore, certain blocks have a second implementation with a graphical

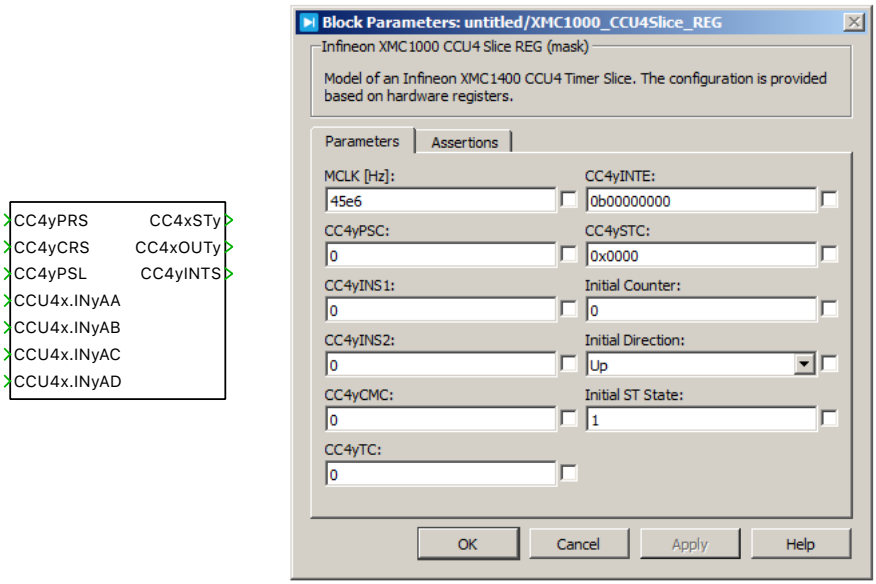
user interface (GUI) that automatically determines the register configurations based on text-based parameter selections.

Subsequent sections describe the PLECS peripheral components in detail and highlight modeling assumptions and limitations. When documenting peripheral register settings, the following color coding is used:

1. **Grey** (dark shading): No effect on the model behavior
2. **Green** (light shading): Register cell affects the behavior of the model

CCU 4 Single Timer Slice (Compare Mode)

The PLECS peripheral library provides two blocks for a single timer slice of the Infineon XMC1xxx Capture/Compare Unit 4 used in compare mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer slice model for compare mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Model overview

The block presented in this documentation models a single slice of the Infineon XMC1xxx Capture/Compare Unit 4. It is focussed on the compare mode of the module and therefore implements a subset of the features available on the hardware relevant for the control of a power converter or a drive system. Assumptions made during modeling as well as limitations and simplifications are described in the next sections.

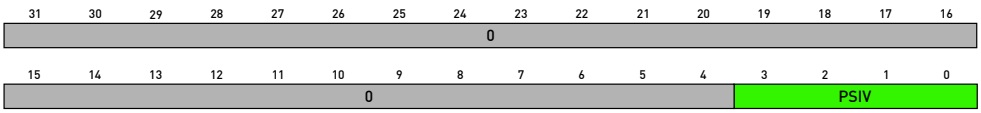
Timer Slice Core Functions

The core timer of the timer slice consists of a 16-bit counter that can be used either in Edge-aligned or Center-aligned mode. The single shot mode is not supported. The counter is assumed to run continuously which means that the start and stop functionality is not part of the model. For simplicity, the complex shadow transfer state machine is omitted. The shadow transfer for compare and period registers is done with the synchronization events as described below. An immediate update is not supported which majorly increases the efficiency of the model.

The counter time base is defined by a prescaled clock period T_{tclk}. The period of this clock depends on the counter clock frequency $f_{ccu4} = M\_CLK$ and the prescaler register *CC4yPSC.PSIV*, both configurable in the mask, as follows:

$$T_{tclk} = \frac{CC4yPSC.PSIV + 1}{f_{ccu4}}$$

The prescaler control register is shown below.



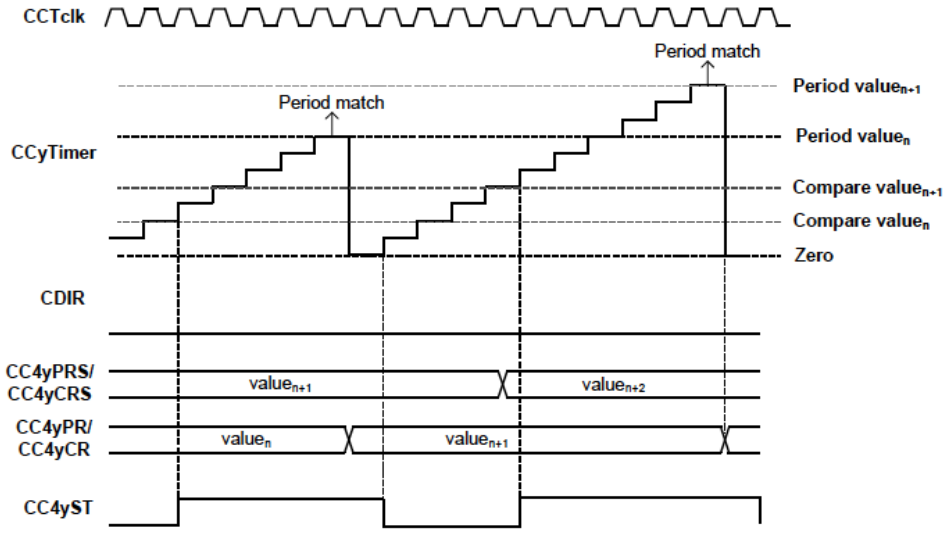
Prescaler Control Register

The *PSIV* field defines the prescaler used for the counter time base.

- 0000 - f_{ccu4}
- 0001 - $f_{ccu4}/2$
- ...
- 1111 - $f_{ccu4}/32768$

Because the floating prescaler mode is not supported, *PVAL* = *PSIV* is always valid. Therefore the field *CC4yTC.FPE* needs to stay cleared.

In Edge-aligned mode the counter is always incremented until it matches the internal period register *PR*. When it reaches 1, the *CC4yST* status bit is set to passive level. With the $Counter = CR + 1$ event, it is set to active level.



Edge-aligned mode [1]

Note that the transfer from the shadow register values *PRS*/*CRS* to the internal registers *PR*/*CR* is synched to the counter overflow. Related to the model, this corresponds to the *PRS*/*CRS* input terminals being sampled with the instants of the counter overflow.

In Edge-aligned mode the pwm period can be calculated by

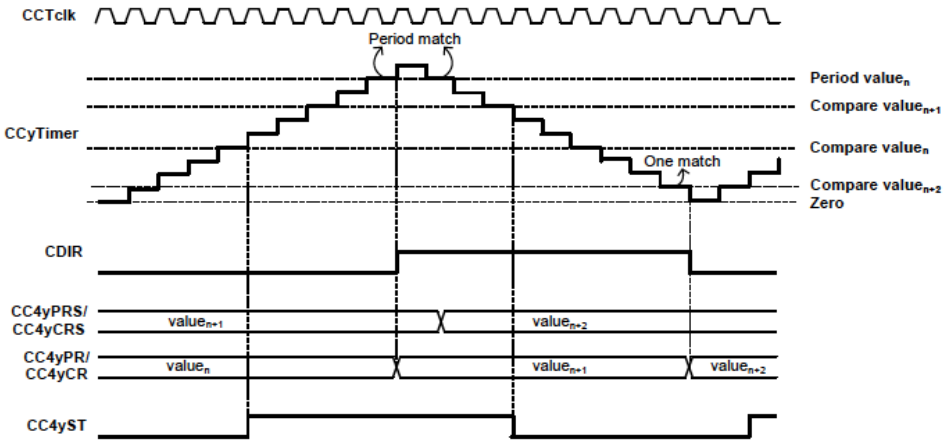
$$T_{per} = T_{tclk} \cdot (PR + 1)$$

and the pwm dutycycle is defined by

$$DC = \frac{CR}{PR + 1}$$

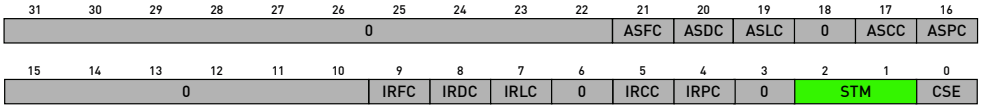
The initial counter value and for center-aligned mode also the initial counter direction can be set in the component mask.

In Center-aligned mode the timer counts up to *PR+1*, inverts its counting direction and counts to zero, where it starts counting up again. The *CC4yST* status bit is set active with the $Counter = CR + 1$ while counting up. It is set to passive with the $Counter = CR - 1$ event while counting down.



Center-aligned mode [1]

The internal registers are updated with the $Counter = PR + 1$ (period match) event and/or with the $Counter = 0$ (one match) event, which depends on the configuration in the shadow transfer control register.



Shadow Transfer Control Register

The field *CC4ySTC.STM* only has an influence in Center-aligned mode and defines the shadow transfer events.

- 00 - Shadow transfer is done in Period Match and One Match
- 01 - Shadow transfer is done only in Period Match (not supported)
- 10 - Shadow transfer is done only in One Match
- 11 - Reserved (not supported)

Note that the period match only setting is not supported by the model due to internal limitations.

In Center-aligned mode the pwm period can be calculated by

$$T_{per} = T_{tclk} \cdot (PR + 1) \cdot 2$$

and the pwm dutycycle is defined by

$$DC = \frac{CR}{PR + 1}$$

The timer counting mode can be set using the slice timer control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MCME	EMT	EMS	TRPSW	TRPSE	0			TRAPE	FPE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIM	DITHE		CCS	SCE	STRM	ENDM		0	CAPC		ECM	CMOD	CLST	TSSM	TCM

Slice Timer Control Register

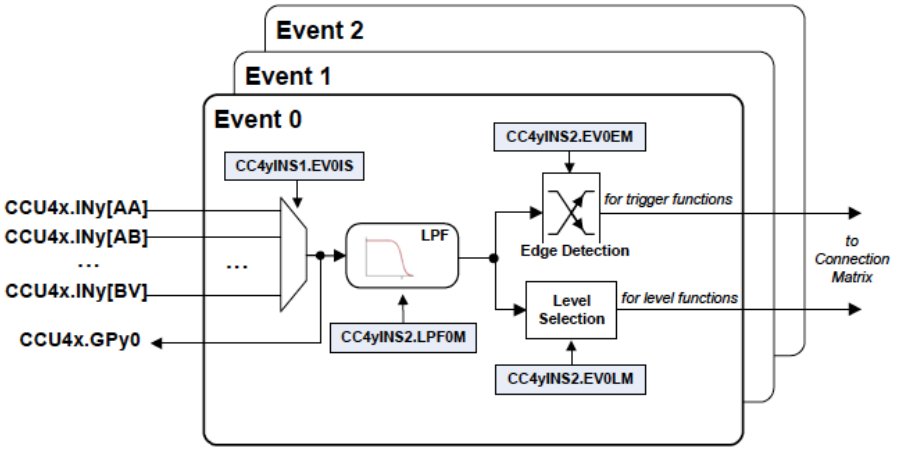
The *TCM* field defines the counter mode.

- 0 - Edge-aligned mode
- 1 - Center-aligned mode

Note that this counter slice implementation only models the compare behavior and therefore *CC4yTC.CMOD* needs to be set to 0. The register fields *TRPSE, TRAPE, EMS, EMT* are related to output path functions and are described in the corresponding section.

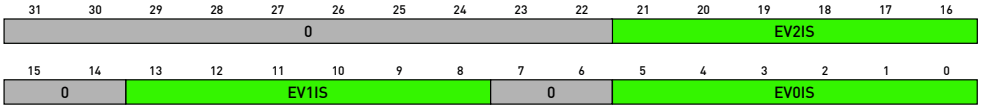
Timer Slice Input Path

The timer slice has 28 input signals that are used to generate 3 events applied to control several functions inside the timer kernel. With the input selector below the user is able to select a specific signal as an event source and to configure the signal conditions invoking it.



Slice Input Selector Diagram [1]

The input selector for all three events is configured via the two input selector configuration registers *CC4yINS1* and *CC4yINS2*.

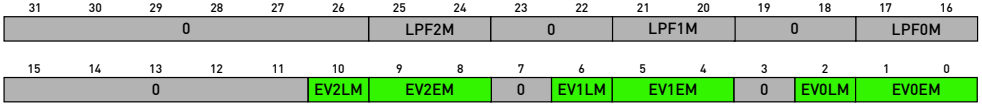


Input Selector Configuration Register 1

The field *EVxIS* is used to choose an input as the source for the related event.

- 00 - CCU4x.INyAA
- 01 - CCU4x.INyAB
- 10 - CCU4x.INyAC
- 11 - CCU4x.INyAD

Note that the timer slice model only has 4 available signals to keep the amount of input signals in a reasonable limit. *EVxIS* values higher than *0b11* are not supported.



Input Selector Configuration Register 2

Because the timer kernel provides edge and level sensitive functions, the input selector provides 2 outputs for each event. The field *EVxEM* defines the edge type invoking an edge sensitive function.

- 00 - No action
- 01 - Signal active on rising edge
- 10 - Signal active on falling edge
- 11 - Signal active on both edges

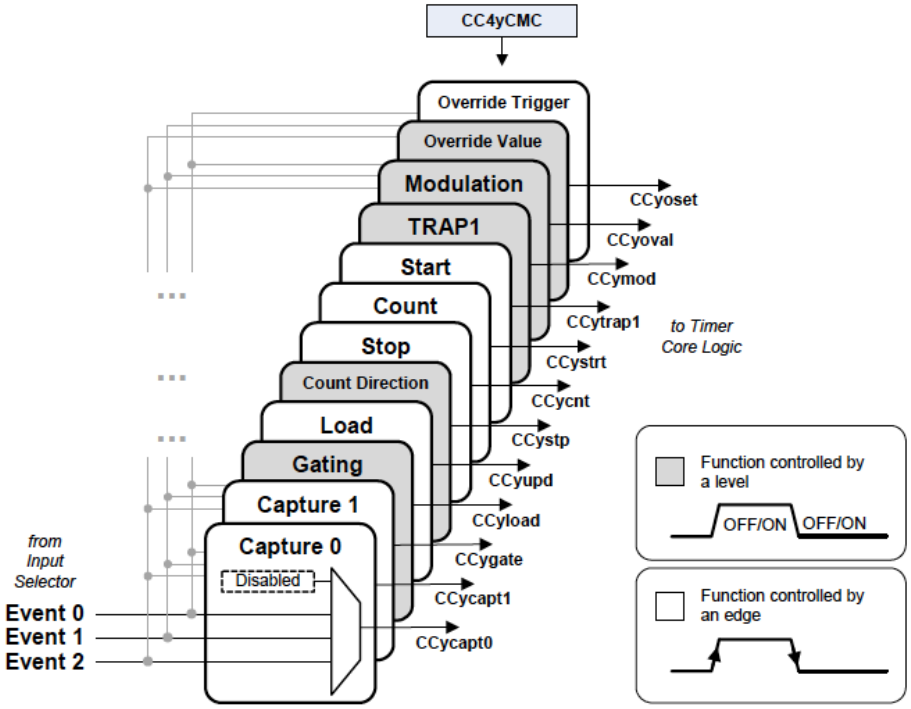
The field *EVxLM* defines the active level for a level sensitive function.

- 0 - Active on high level
- 1 - Active on low level

Note that the low pass filtering is not implemented in the model and therefore all *LPFxM* fields have no influence on the event generation.

Slice Connection Matrix

The timer kernel provides user configured functions which can have an influence on the pwm output path. The figure below shows all available functions.



Slice Connection Matrix Diagram [1]

The coloring specifies if the function is level or edge controlled. The timer slice model supports the Override, Modulation and TRAP1 functions. The connection between the events and the functions is done via the *CC4yCMC* register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											TCE	MOS		TS	OFS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTS		LDS		UDS		GATES		CAP1S		CAP0S		ENDS		STRTS	

Connection Matrix Control Register

The bit *OFS* selects the events used for the override function.

- 0 - Override functionality disabled
- 1 - Status Bit Override Trigger connected to Event 1; Status bit override value connected to Event 2.

The bit *TS* connects the Trap function.

- 0 - Trap function disabled
- 1 - Trap function connected to Event 2

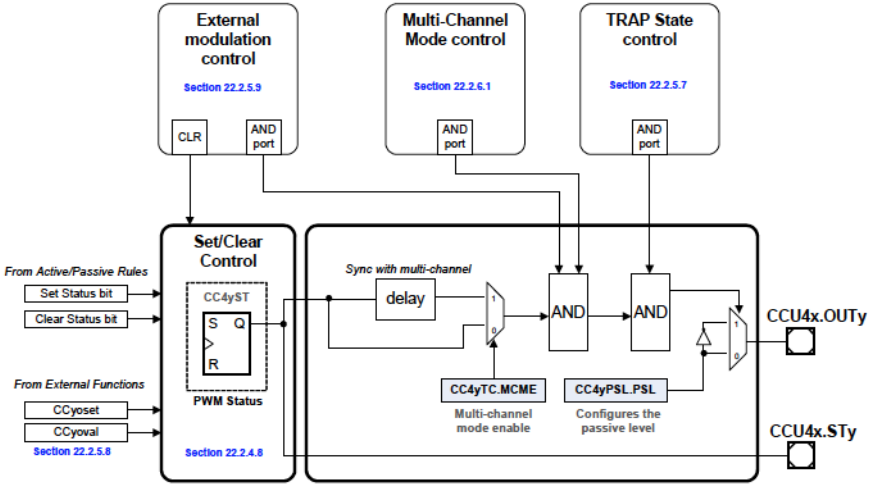
Note that the *CC4yTC.TRAPE* bit needs to be set to enable the trap function.

The field *MOS* selects the event connected to the modulation function.

- 00 - Modulation function deactivated
- 01 - Modulation function connected to Event 0
- 10 - Modulation function connected to Event 1
- 11 - Modulation function connected to Event 2

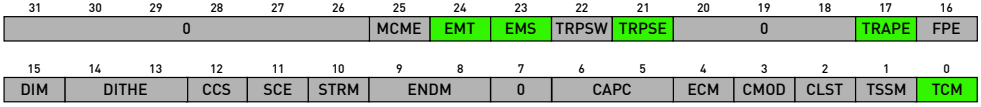
Timer Slice Output Path

The output path of the timer slice module generates a status and an output signal and is shown in the figure below.



PWM Output Path [1]

The timer slice model implements the active/passive rules, the external override function as well as the external modulation and trap state control. The multi-channel mode control is not supported. The external modulation and trap state control behavior can be configured with the *CC4yTC* register.



Slice Timer Control Register

The bit *TRAPE* enables the Trap function.

- 0 - Trap function has no effect on the output
- 1 - Trap function affects the output

The bit *TRAPSE* enables a synchronous exit from trap state.

- 0 - Exiting from TRAP state is not synchronized with the PWM signal
- 1 - Exiting from TRAP state is synchronized with the PWM signal

Note that an exit of the trap state via software is not supported and therefore the bit *CC4yTC.TRPSW* needs to stay cleared.

The bit *EMS* enables a synchronization of the modulation function with the pwm period.

- 0 - External Modulation function is not synchronized with the PWM signal
- 1 - External Modulation function is synchronized with the PWM signal

The bit *EMT* controls the type of the external modulation.

- 0 - External Modulation function is clearing the ST bit
- 1 - External Modulation function is gating the outputs

For more detailed information about the different functions and their behavior please refer to [1].

The *CC4yPSL* input defines the passive level of the output signals. It can be updated immediately during the simulation. The initial *ST* value can be set in the component mask.

Timer Slice Advanced Functions

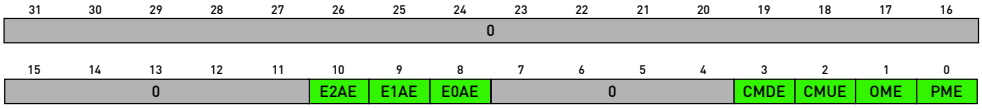
The hardware module provides additional features like pwm dithering, timer concatenation or an external access to the counting direction. Because those features typically are not used in a simulation of a power converter or a drive control system, they are not reflected in the model.

Timer Slice Interrupt generation

The timer slice block models the interrupt feature of the hardware module. The interrupt status bits of the *CC4yINTS* register can be accessed via the *CC4yINTS* output which is arranged as follows:

{PMUS, OMDS, CMUS, CMDS, E0AS, E1AS, E2AS}.

The *CC4yINTE* register can be applied to activate the different interrupt pulses by writing a 1 to the corresponding field.



Slice Timer Interrupt Enable Control Register

Timer Slice Flag Signals

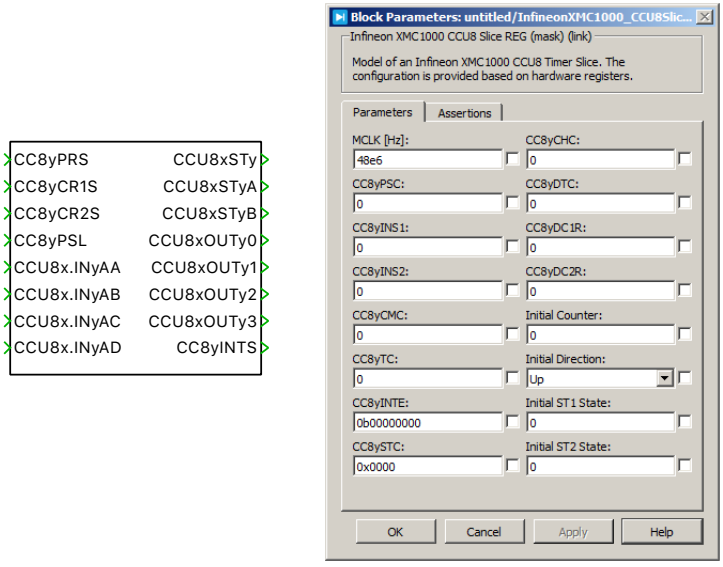
The timer slice model provides access to a *FLAGS* component signal that provides access to the following internal signals.

- Counter Value
- CRS Hit Event
- PRS Hit Event
- Zero Hit Event
- Counter Direction
- Status Bit Override Trigger
- Status Bit Override Level
- Trap Status
- Modulation Status

Those signals can be used to further analyze the timer and event behavior of the module.

CCU 8 Single Timer Slice (Compare Mode)

The PLECS peripheral library provides two blocks for a single timer slice of the Infineon XMC1xxx Capture/Compare Unit 8 used in compare mode. One block has a register-based configuration mask and a second block features a GUI. In both cases, you should distinguish between registers configured in the parameter mask and inputs to the block. Mask parameters are fixed (static) during a simulation and correspond to the configurations which the embedded software uses during the initialization phase. Inputs are dynamically changeable while the simulation is running. The fixed configuration can be entered either using a register-based approach or a GUI, while the dynamic values supplied at the inputs must correspond to raw register values. The figure below shows the block and its parameters for the register-based version.



Register-based Timer slice model for compare mode

As depicted above, the block can be configured directly using the registers of the hardware module, making it possible to exactly mirror the configuration applied to the target. Also as shown, either hexadecimal, decimal or binary representation can be used to enter the configuration.

Model overview

The block presented in this documentation models a single slice of the Infineon XMC1xxx Capture/Compare Unit 8. It is focussed on the compare mode of the module and therefore implements a subset of the features available on the hardware relevant for the control of a power converter or a drive system. Assumptions made during modeling as well as limitations and simplifications are described in the next sections.

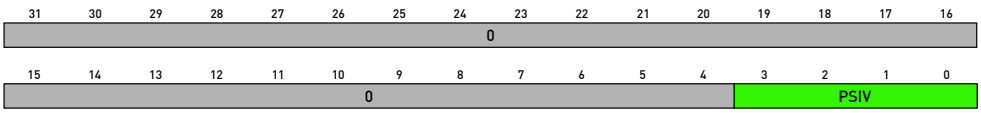
Timer Slice Core Functions

The core timer of the timer slice consists of a 16-bit counter that can be used either in Edge-aligned or Center-aligned mode. The single shot mode is not supported. The counter is assumed to run continuously which means that the start and stop functionality is not part of the model. For simplicity, the complex shadow transfer state machine is omitted. The shadow transfer for compare and period registers is done with the synchronization events as described below. An immediate update is not supported which majorly increases the efficiency of the model.

The counter time base is defined by a prescaled clock period T_{tclk}. The period of this clock depends on the counter clock frequency $f_{ccu8} = M\_CLK$ and the prescaler register *CC8yPSC.PSIV*, both configurable in the mask, as follows:

$$T_{tclk} = \frac{CC8yPSC.PSIV + 1}{f_{ccu8}}$$

The prescaler control register is shown below.



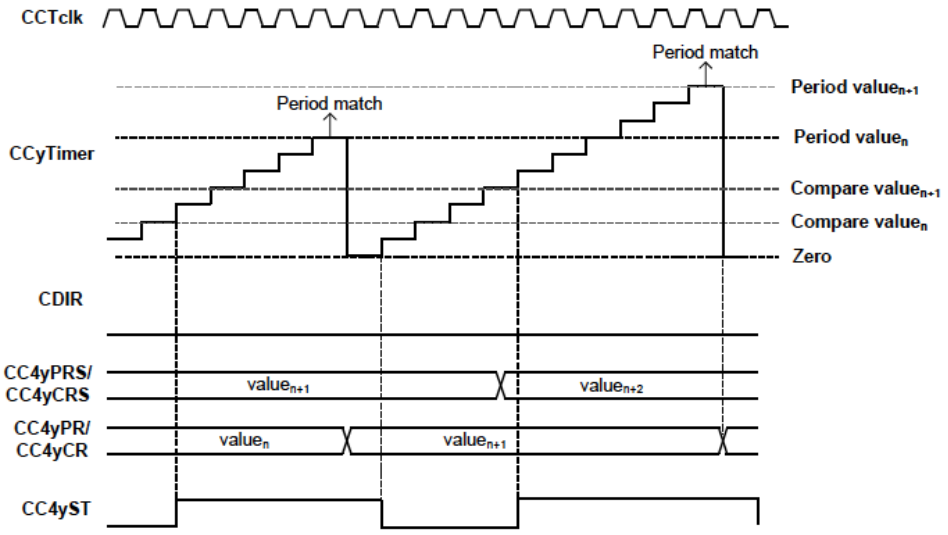
Prescaler Control Register

The *PSIV* field defines the prescaler used for the counter time base.

- 0000 - f_{ccu8}
- 0001 - $f_{ccu8}/2$
- ...
- 1111 - $f_{ccu8}/32768$

Because the floating prescaler mode is not supported, *PVAL* = *PSIV* is always valid. Therefore the field *CC8TC.FPE* needs to stay cleared.

In Edge-aligned mode the counter is always incremented until it matches the internal period register *PR*.



Edge-aligned mode [2]

Note that the transfer from the shadow register values *PRS*/*CRS* to the internal registers *PR*/*CR* is synched to the counter overflow. Related to the model, this corresponds to the *PRS*/*CRS* input terminals beeing sampled with the instants of the counter overflow.

In Edge-aligned mode the pwm period can be calculated by

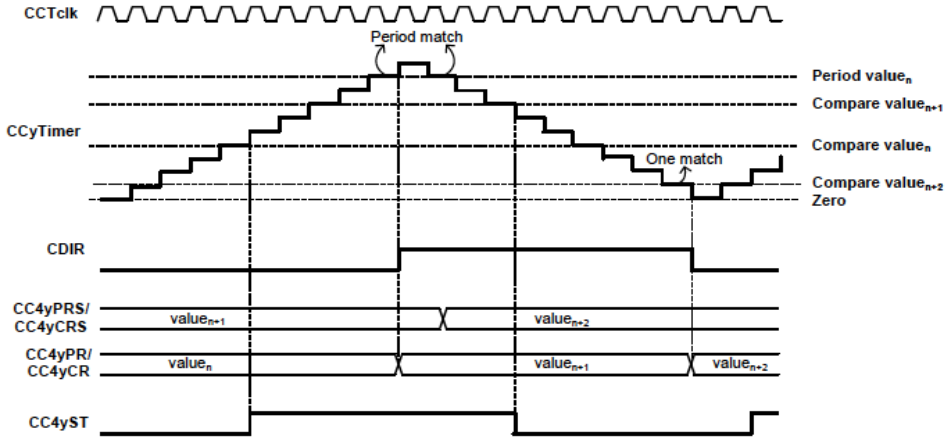
$$T_{per} = T_{tclk} \cdot (PR + 1)$$

and the pwm dutycycle is defined by

$$DC = \frac{CR}{PR + 1}$$

The initial counter value can be set in the component mask.

In Center-aligned mode the timer counts up to *PR+1*, inverts its counting direction and counts to zero, where it starts counting up again.



Center-aligned mode [2]

The internal registers are updated with the $Counter = PR + 1$ (period match) event and/or with the $Counter = 0$ (one match) event, which depends on the configuration in the shadow transfer control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										ASFC	ASDC	ASLC	0	ASCC	ASPC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						IRFC	IRDC	IRLC	0	IRCC	IRPC	0	STM		CSE

Shadow Transfer Control Register

The field *CC8ySTC.STM* only has an influence in Center-aligned mode and defines the shadow transfer events.

- 00 - Shadow transfer is done in Period Match and One Match
- 01 - Shadow transfer is done only in Period Match (not supported)
- 10 - Shadow transfer is done only in One Match
- 11 - Reserved (not supported)

Note that the period match only setting is not supported by the model due to internal limitations.

In Center-aligned mode the pwm period can be calculated by

$$T_{per} = T_{tclk} \cdot (PR + 1) \cdot 2$$

and the pwm dutycycle is defined by

$$DC = \frac{CR}{PR + 1}$$

The initial counter value and the initial counter direction can be set in the component mask. The timer counting mode can be configured via the slice timer control register.

31	30 29	28 27	26	25	24	23	22	21	20	19	18	17	16
0	STOS	EME	MCME2	MCME1	EMT	EMS	TRPSW	TRPSE	TRAPE3	TRAPE2	TRAPE1	TRAPE0	FPE

15	14 13	12	11	10	9 8	7	6 5	4	3	2	1	0
DIM	DITHE	CCS	SCE	STRM	ENDM	0	CAPC	ECM	CMOD	CLST	TSSM	TCM

Slice Timer Control Register

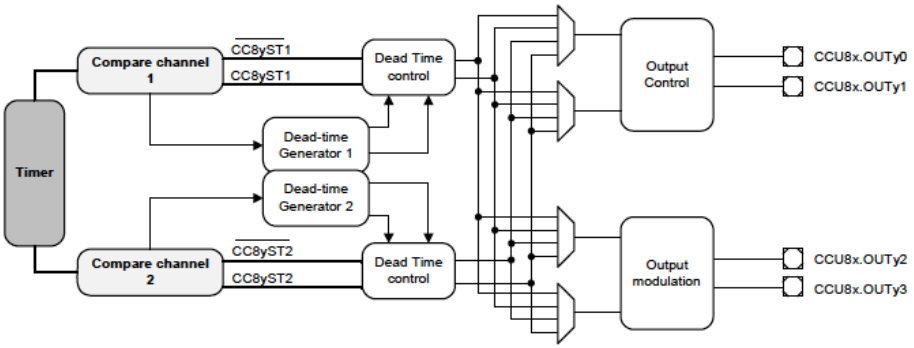
The *TCM* field defines the counter mode.

- 0 - Edge-aligned mode
- 1 - Center-aligned mode

Note that this counter slice implementation only models the compare behavior and therefore *CC8yTC.CMOD* needs to be set to 0. The register fields *TRAPEx, TRPSE, EMS, EMT, EME and STOS* are related to output path functions and are described in the corresponding section.

Timer Slice Compare Modes and ST generation

Each timer slice of the CCU8 unit has two compare channels which both generate a complementary set of status bits.



Slice Compare Channel Diagram [2]

Each channel further contains a dead time generator which is applied to prevent short circuiting in power electronic devices. The output path shown on the right enables a configurable mapping of the status bits to the outputs *Outy0 - Outy3* and adds additional output control functions.

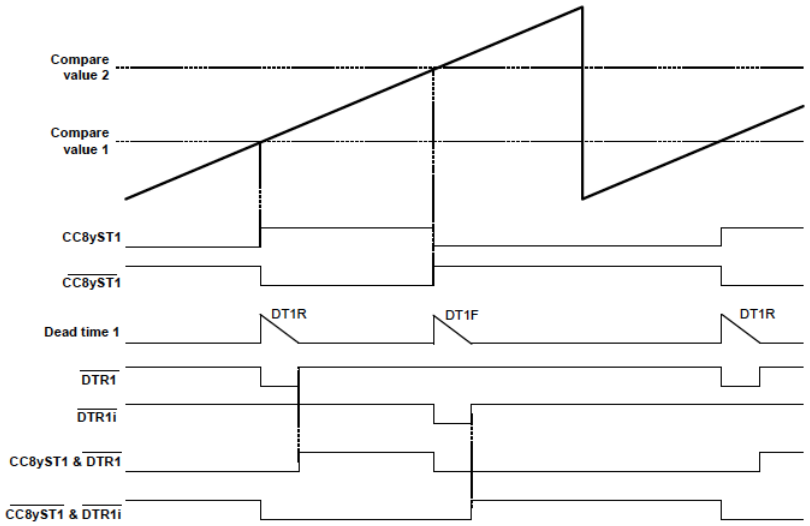
The compare channels can be used for symmetric and asymmetric pwm generation configured by the register field *CC8yCHC.ASE*. The logic applied for the status bit generation in the different modes is summarized in the table below.

Event/Mode	Edge Sym.	Edge Asym.	Center Sym.	Center Asym.
Set ST1	CR = CR1S	CR = CR1S	CR = CR1S CDIR = 0	CR = CR1S CDIR = 0
Clear ST1	CR = PRS	CR = CR2S	CR = CR1S CDIR = 1	CR = CR2S CDIR = 1
Set ST2	CR = CR2S	CR = CR2S	CR = CR2S CDIR = 0	CR = CR2S CDIR = 0
Clear ST2	CR = PRS	CR = PRS	CR = CR2S CDIR = 1	CR = CR2S CDIR = 1

Note that a status change is always delayed by one counter clock cycle period. In asymmetrical edge-aligned mode ST1 stays always 0 if $CR2S < CR1S$.

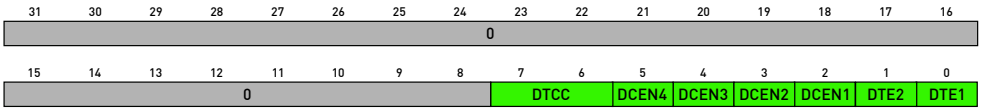
Timer Slice Dead Time Generator

The timer slice has a dead time generator for every compare channel. This module is used to delay the switching edges of a complementary output signal to prevent short circuits in a power stage. The figure below shows a dead time generation for compare channel 1 in asymmetric, edge-aligned mode.



Timer Slice Dead Time Generation [2]

Note that the positive edge of *ST1* is delayed by a time *DT1R* while the positive edge of the inverted status bit is delayed by the time *DT1F*. The dead time generation is configured via the *CC8y.DTC* and *CC8y.DCxR* registers.

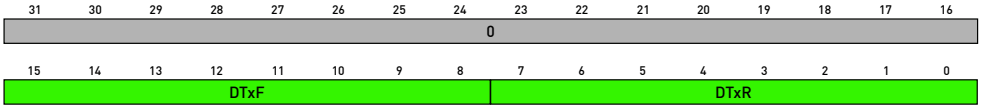


Slice Dead Time Control Register

The deadtime module of a compare channel needs to be enabled with the register cells *DTEx*. Further its possible to separately enable/disable the dead time generation for each single channel. For example, the dead time generation of the *ST1* channel is activated by setting the bit *DCEN1*. The bit *DCEN2* activates the dead time for the inverted *ST1* channel.

The register field *DTCC* is used to configure the clock frequency for the internal dead time counters.

- 00 - $f_{dtg\_clk} = f_{tclk}$
- 01 - $f_{dtg\_clk} = f_{tclk}/2$
- 10 - $f_{dtg\_clk} = f_{tclk}/4$
- 11 - $f_{dtg\_clk} = f_{tclk}/8$



Slice Dead Time Value Register

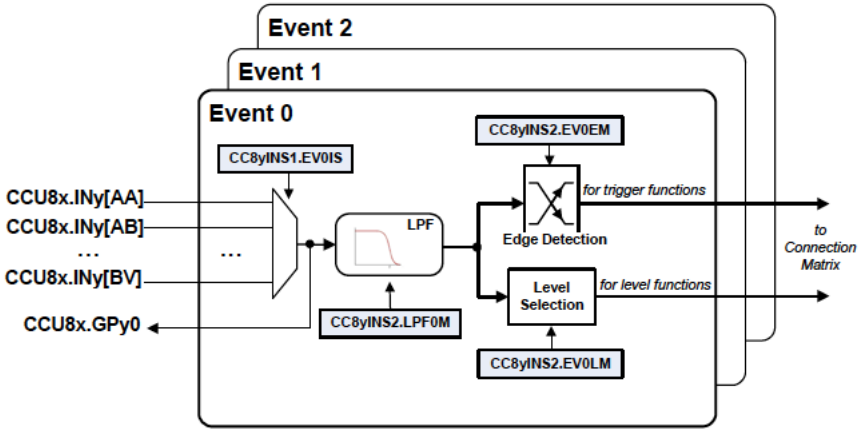
The field *DTxR* defines the delay for the positive edge of the *STx* signal. The field *DTxF* defines the delay for the positive edge of the inverted *STx* signal.

The dead time applied to the positive edge of the non-inverted ST1 i.e. can be calculated with

$$T_{dead\_ST1} = \frac{CC8yDC1R.DT1R}{f_{dtg\_clk}}$$

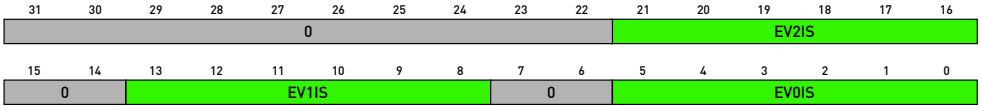
Timer Slice Input Path

The timer slice has 28 input signals that are used to generate 3 events applied to control several functions inside the timer kernel or the output path. With the input selector below the user is able to select a specific signal as an event source and to configure the signal conditions invoking it.



Slice Input Selector Diagram [2]

The input selector for all three events is configured via the two input selector configuration registers *CC8yINS1* and *CC8yINS2*.

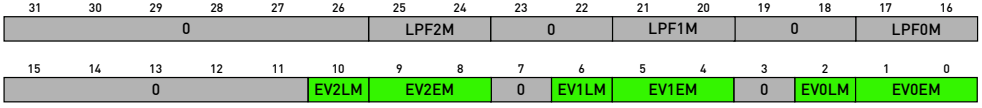


Input Selector Configuration Register 1

The field *EVxIS* is used to choose an input as the source for the related event.

- 00 - CCU8x.INyAA
- 01 - CCU8x.INyAB
- 10 - CCU8x.INyAC
- 11 - CCU8x.INyAD

Note that the timer slice model only has 4 available signals to keep the amount of input signals in a reasonable limit. *EVxIS* values higher than *0b11* are not supported.



Input Selector Configuration Register 2

Because the timer kernel provides edge and level sensitive functions, the input selector provides 2 outputs for each event. The field *EVxEM* defines the edge type invoking an edge sensitive function.

- 00 - No action
- 01 - Signal active on rising edge
- 10 - Signal active on falling edge
- 11 - Signal active on both edges

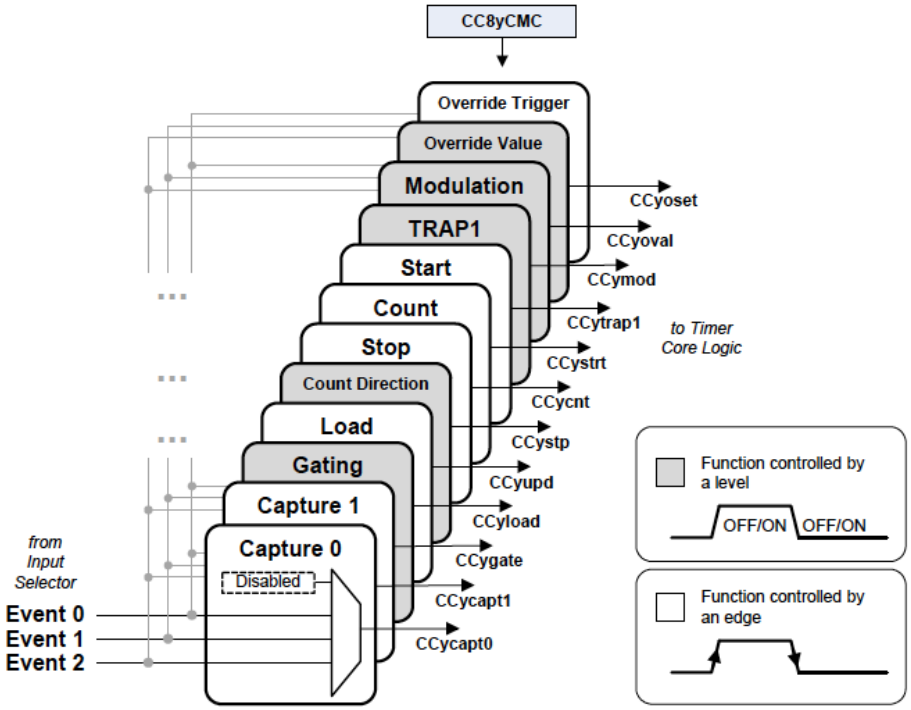
The field *EVxLM* defines the active level for a level sensitive function.

- 0 - Active on high level
- 1 - Active on low level

Note that the low pass filtering is not implemented in the model and therefore all *LPFxM* fields have no influence on the event generation.

Slice Connection Matrix

The timer kernel provides user configured functions which can have an influence on the pwm output path. The figure below shows all available functions.



Slice Connection Matrix Diagram [2]

The coloring specifies if the function is level or edge controlled. The timer slice model supports the Override, Modulation and TRAP1 functions. The connection between the events and the functions is done via the *CC8yCMC* register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											TCE	MOS		TS	OFS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNTS		LDS		UDS		GATES		CAP1S		CAP0S		ENDS		STRTS	

Connection Matrix Control Register

The bit *OFS* selects the events used for the override function.

- 0 - Override functionality disabled
- 1 - Status Bit Override Trigger connected to Event 1; Status bit override value connected to Event 2.

The bit *TS* connects the Trap function.

- 0 - Trap function disabled
- 1 - Trap function connected to Event 2

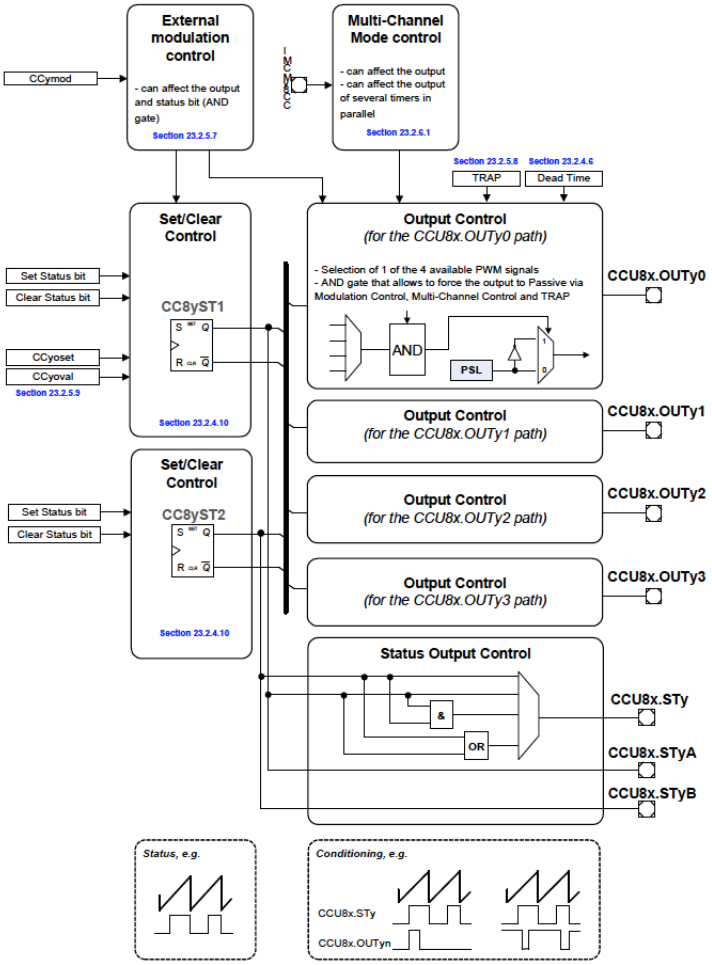
Note that the *CC8yTC.TRAPE* bit needs to be set to enable the trap function.

The field *MOS* selects the event connected to the modulation function.

- 00 - Modulation function deactivated
- 01 - Modulation function connected to Event 0
- 10 - Modulation function connected to Event 1
- 11 - Modulation function connected to Event 2

Timer Slice Output Path

The Set/Clear control of the timer slice module generates 2 pairs of complementary status bits. Those bits can selectively be forwarded to 7 available outputs of the timer slice output path shown below.

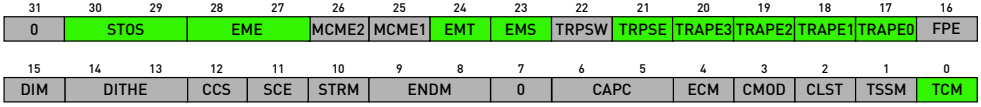


PWM Output Path [2]

The output path model implements the external status bit override option as well as the external modulation and trap state control features of the hard-

ware peripheral. The multi-channel mode control is not supported. The output and status output control blocks implement a selective connection of the different status bits to the output channels. Further its possible to define the passive/active level for each output channel separately.

The external modulation and trap state features as well as the state output control is configured with the *CC8yTC* register.



Slice Timer Control Register

The bit *TRAPEx* enables the Trap function for output channel x.

- 0 - Trap function has no effect on the output
- 1 - Trap function affects the output

The bit *TRAPSE* enables a synchronous exit from trap state.

- 0 - Exiting from TRAP state is not synchronized with the PWM signal
- 1 - Exiting from TRAP state is synchronized with the PWM signal

Note that an exit of the trap state via software is not supported and therefore the bit *CC8yTC.TRPSW* needs to stay cleared.

The bit *EMS* enables a synchronization of the modulation function with the pwm period.

- 0 - External Modulation function is not synchronized with the PWM signal
- 1 - External Modulation function is synchronized with the PWM signal

The bit *EMT* controls the type of the external modulation.

- 0 - External Modulation function is clearing the ST bit
- 1 - External Modulation function is gating the outputs

The field *EME* defines which compare channels are affected by the external modulation.

- 00 - External Modulation does not affect any channel
- 01 - External Modulation only applied on channel 1
- 10 - External Modulation only applied on channel 2
- 11 - External Modulation applied on both channels

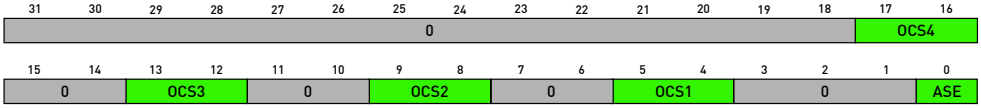
For more detailed information about the different functions and their behavior please refer to [2].

The field *STOS* configures to which channel the output *CCU8x.STy* is mapped.

- 00 - CC8yST1 forward to CCU8x.STy
- 01 - CC8yST2 forward to CCU8x.STy
- 10 - CC8yST1 AND CC8yST2 forward to CCU8x.STy
- 11 - CC8yST1 OR CC8yST2 forward to CCU8x.STy

Please note that the outputs *CCU8x.STA*, *CCU8x.STB* and *CCU8x.STy* directly represent the state of the flip-flops and therefore do not contain dead time insertion.

Each output control path can freely select from the four status bits. This is configured by the *CC8yCHC* register.



Channel Control Register

The field *OCS1* defines the status bit used as the source for *CCU8x.OUTy0*.

- 00 - CC8yST1 signal path is connected to the CCU8x.OUTy0
- 01 - Inverted CC8yST1 signal path is connected to the CCU8x.OUTy0
- 10 - CC8yST2 signal path is connected to the CCU8x.OUTy0
- 11 - Inverted CC8yST2 signal path is connected to the CCU8x.OUTy0

The field *OCS2* defines the status bit used as the source for *CCU8x.OUTy1*.

- 00 - Inverted CC8yST1 signal path is connected to the CCU8x.OUTy1
- 01 - CC8yST1 signal path is connected to the CCU8x.OUTy1
- 10 - Inverted CC8yST2 signal path is connected to the CCU8x.OUTy1
- 11 - CC8yST2 signal path is connected to the CCU8x.OUTy1

The field *OCS3* defines the status bit used as the source for *CCU8x.OUTy2*.

- 00 - CC8yST2 signal path is connected to the CCU8x.OUTy2
- 01 - Inverted CC8yST2 signal path is connected to the CCU8x.OUTy2

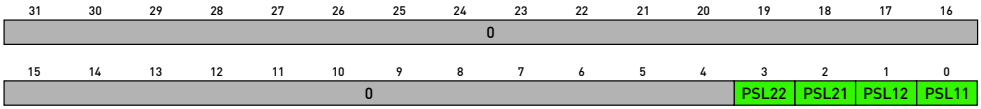
- 10 - CC8yST1 signal path is connected to the CCU8x.OUTy2
- 11 - Inverted CC8yST1 signal path is connected to the CCU8x.OUTy2

The field *OCS4* defines the status bit used as the source for *CCU8x.OUTy3*.

- 00 - Inverted CC8yST2 signal path is connected to the CCU8x.OUTy3
- 01 - CC8yST2 signal path is connected to the CCU8x.OUTy3
- 10 - Inverted CC8yST1 signal path is connected to the CCU8x.OUTy3
- 11 - CC8yST1 signal path is connected to the CCU8x.OUTy3

Please note that all four fields have a different resulting connection for the same setting.

The *CC8yPSL* input defines the passive level of the output signals.



Passive Level Config Register

If a bit in the register is set, the corresponding outputs passive level is active low. The input is updated immediately during the simulation. The initial *STx* values can be set in the component mask.

Timer Slice Advanced Functions

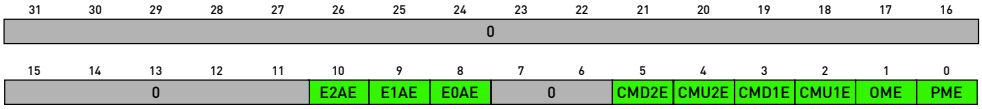
The hardware module provides additional features like pwm dithering, timer concatenation or an external access to the counting direction. Because those features typically are not used in a simulation of a power converter or a drive control system, they are not reflected in the model.

Timer Slice Interrupt generation

The timer slice block models the interrupt feature of the hardware module. The interrupt status bits of the *CC8yINTS* register can be accessed via the *CC8yINTS* output which is arranged as follows:

{PMUS, OMDS, CMU1S, CMD1S, CMU2S, CMD2S, E0AS, E1AS, E2AS}.

The *CC8yINTE* register can be applied to activate the different interrupt pulses by writing a 1 to the corresponding field.



Slice Timer Interrupt Enable Control Register

Timer Slice Flag Signals

The timer slice model provides access to a *FLAGS* component signal that provides access to the following internal signals.

- Counter Value
- CR1S Hit Event
- CR2S Hit Event
- PRS Hit Event
- Zero Hit Event
- Counter Direction
- Status Bit Override Trigger
- Status Bit Override Level
- Trap Status
- Modulation Status

Those signals can be used to further analyze the timer and event behavior of the module.

Reference

1 - Literature Source: Infineon Reference Manual CCU4 [v2.3]

2 - Literature Source: Infineon Reference Manual CCU8 [v2.3]

10

Components by Category

This chapter lists the blocks of the PIL library by category.

Peripheral Blocks Infineon XMC1000

Infineon XMC1000 CCU4 Slice Compare Mode GUI	Provide a CCU4 timer slice model for pwm generation with graphical user interface configuration
Infineon XMC1000 CCU4 Slice Compare Mode REG	Provide a CCU4 timer slice model for pwm generation with register based configuration
Infineon XMC1000 CCU8 Slice Compare Mode GUI	Provide a CCU8 timer slice model for pwm generation with graphical user interface configuration
Infineon XMC1000 CCU8 Slice Compare Mode REG	Provide a CCU8 timer slice model for pwm generation with register based configuration

Peripheral Blocks TI C2000

TI C2000 ADC Type 2 GUI	Provide an ADC module model with graphical user interface configuration
TI C2000 ADC Type 2 REG	Provide an ADC module model with register based configuration
TI C2000 ADC Type 3 GUI	Provide an ADC module model with graphical user interface configuration
TI C2000 ADC Type 3 REG	Provide an ADC module model with register based configuration

TI C2000 ADC Type 3 Simplified	Provide a simplified ADC module with single sequential or simultaneous sampling
TI C2000 ADC Type 4 GUI	Provide an ADC module model with graphical user interface configuration
TI C2000 ADC Type 4 REG	Provide an ADC module model with register based configuration
TI C2000 eCAP Type 0 APWM GUI	Provide a model of an eCAP module operate in APWM mode with graphical user interface configuration
TI C2000 eCAP Type 0 CAP GUI	Provide a model of an eCAP module operate in capture mode with graphical user interface configuration
TI C2000 eCAP Type 0 CAP REG	Provide a model of an eCAP module operate in capture mode with register based configuration
TI C2000 ePWM Type 1 Configurator	Provide a helper block for generation of AQCTLx and AQCSFRC registers
TI C2000 ePWM Type 1 GUI	Provide an ePWM module model with graphical user interface configuration
TI C2000 ePWM Type 1 REG	Provide an ePWM module model with register based configuration
TI C2000 ePWM Type 4 Configurator	Provide a helper block for generation of AQCTLx, AQCTLx2, and AQCSFRC registers
TI C2000 ePWM Type 4 GUI	Provide an ePWM module model with graphical user interface configuration
TI C2000 ePWM Type 4 REG	Provide an ePWM module model with register based configuration
TI C2000 eQEP Type 0 GUI	Provide an eQEP module model with graphical user interface configuration
TI C2000 eQEP Type 0 REG	Provide an eQEP module model with register based configuration

Peripheral Blocks STM32 F0

STM32 F0 ADC GUI	Provide an ADC module model with graphical user interface configuration
STM32 F0 ADC REG	Provide an ADC module model with register based configuration
STM32 F0 Timer Output Configurator	Provide a helper block for generation of OcxM and CCER registers
STM32 F0 Timer Output GUI	Provide a timer module model for pwm generation with graphical user interface configuration
STM32 F0 Timer Output REG	Provide a timer module model for pwm generation with register based configuration

Peripheral Blocks STM32 F1

STM32 F1 ADC GUI	Provide an ADC module model with graphical user interface configuration
STM32 F1 ADC REG	Provide an ADC module model with register based configuration
STM32 F1 Timer Output Configurator	Provide a helper block for generation of OcxM and CCER registers
STM32 F1 Timer Output GUI	Provide a timer module model for pwm generation with graphical user interface configuration
STM32 F1 Timer Output REG	Provide a timer module model for pwm generation with register based configuration

Peripheral Blocks STM32 F3

STM32 F3 ADC GUI	Provide an ADC module model with graphical user interface configuration
STM32 F3 ADC REG	Provide an ADC module model with register based configuration
STM32 F3 Timer Output Configurator	Provide a helper block for generation of OcxM and CCER registers

STM32 F3 Timer Output GUI	Provide a timer module model for pwm generation with graphical user interface configuration
STM32 F3 Timer Output REG	Provide a timer module model for pwm generation with register based configuration

Peripheral Blocks STM32 F2/F4

STM32 F2/F4 ADC GUI	Provide an ADC module model with graphical user interface configuration
STM32 F2/F4 ADC REG	Provide an ADC module model with register based configuration
STM32 F2/F4 Timer Output Configurator	Provide a helper block for generation of OcxM and CCER registers
STM32 F2/F4 Timer Output GUI	Provide a timer module model for pwm generation with graphical user interface configuration
STM32 F2/F4 Timer Output REG	Provide a timer module model for pwm generation with register based configuration

Peripheral Blocks Microchip dsPIC33F

MC dsPIC33F MCADC GUI	Provide a motor control ADC module model with graphical user interface configuration
MC dsPIC33F MCADC REG	Provide a motor control ADC module model with register based configuration
MC dsPIC33F MCPWM GUI	Provide a motor control pwm generation with graphical user interface configuration
MC dsPIC33F MCPWM REG	Provide a motor control pwm generation with register based configuration
MC dsPIC33F MCPWMx GUI	Provide a motor control pwm generation with graphical user interface configuration for a single pwm module

11

Component Reference

This chapter lists the contents of the Processor in the Loop Component library in alphabetical order.

Infineon XMC1000 CCU4 Slice Compare Mode GUI

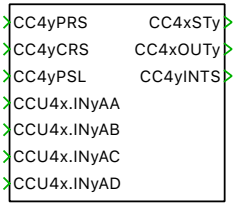
Purpose

High fidelity model of a Infineon CCU4 Timer slice with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / Infineon XMC1000 / CCU

Description



This block efficiently models the behavior of a single Infineon XMC1000 CCU4 timer slice with full timing resolution. The component is focused to the capture mode. Beneath the typical PWM generation it also supports the external override, trap and modulation features. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the Infineon XMC1000 CCU4 timer slice. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “CCU4 Single Timer Slice (Compare Mode)” (on page 279).

Parameters

General

MCLK [Hz] (see page 280)
The base clock of the CCU4 defined in Hz.

CC4yPSC (see page 280)
Defines a clock prescaler.

CC4yTC.TCM (see page 280)
Defines the counter mode.

CC4yTC.TRAPE (see page 287)
Enables trap functionality.

CC4yTC.TRAPSE (see page 287)
Defines trap release behavior.

CC4yTC.EMS (see page 287)
Defines the modulation synchronization behavior.

CC4yTC.EMT (see page 287)
Defines the modulation behavior.

CC4ySTC.STM (see page 280)
Defines the shadow transfer events in center aligned mode.

Initial Counter (see page 280)
Counter initialization.

Initial Direction (see page 280)
Initial direction in up-down-count mode.

Initial State (see page 287)
Initial output state for ST.

Input Selection

CC4yINS1.EVxIS (see page 284)
Specifies input source for event x.

CC4yINS2.EVxEM (see page 284)
Specifies edges used as trigger for event x.

CC4yINS2.EVxLM (see page 284)
Specifies level used for event x.

Connection Matrix

CC4yCMC.OFS (see page 286)
Enables and connects override functionality.

CC4yCMC.TS (see page 286)
Enables and connects trap functionality.

CC4yCMC.MOS (see page 286)
Connects modulation functionality to an event.

Interrupt Enable

CC4yINTE.PME (see page 289)
Enables interrupt for period match event.

CC4yINTE.OME (see page 289)
Enables interrupt for one match event.

CC4yINTE.CMUE (see page 289)
Enables interrupt for compare match event while upcounting.

CC4yINTE.CMDE (see page 289)
Enables interrupt for compare match event while downcounting.

CC4yINTE.ExAE (see page 289)
Enables interrupt for event x detection.

Probe Signals

CC4yPRS
Period Register.

CC4yCRS
Compare Register.

CC4yPSL
Passive Level Register status.

CC4x.INyAA
AA Input Signal status.

CC4x.INyAB
AB Input Signal status.

CC4x.INyAC
AC Input Signal status.

CC4x.INyAD
AD Input Signal status.

CC4xSTy
Status bit.

CC4xOUTy
Output status.

CC4yINTS
Interrupt Status Register status.

CC4yPSC
Prescaler Register status.

CC4yINS1
Input Selector Register 1 status.

CC4yINS2
Input Selector Register 2 status.

CC4yINTE
Interrupt Enable Register status.

CC4yCMC
Connection Matrix Control Register status.

CC4yTC
Slice Timer Control Register status.

CC4ySTC
Shadow Transfer Control Register status.

FLAGS
Flags for further system analysis (see page 289).

Infineon XMC1000 CCU4 Slice Compare Mode REG

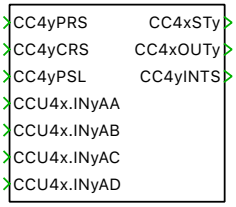
Purpose

High fidelity model of a Infineon CCU4 Timer slice with register based configuration.

Library

Processor in the Loop / Peripherals / Infineon XMC1000 / CCU

Description



This block efficiently models the behavior of a single Infineon XMC1000 CCU4 timer slice with full timing resolution. The component is focused to the capture mode. Beneath the typical PWM generation it also supports the external override, trap and modulation features. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “CCU4 Single Timer Slice (Compare Mode)” (on page 279).

Parameters

MCLK [Hz] (see page 280)
The base clock of the CCU4 defined in Hz.

CC4yPSC (see page 280)
Defines a clock prescaler.

CC4yTC (see page 287)
Slice Timer Control Register.

CC4yINS1 (see page 284)
Input Selector Register 1.

CC4yINS2 (see page 284)
Input Selector Register 2.

CC4yCMC (see page 286)
Connection Matrix Control Register.

CC4yINTE (see page 289)
Interrupt Enable Register.

CC4ySTC (see page 280)
Shadow Transfer Control Register.

Initial Counter (see page 280)
Counter initialization.

Initial Direction (see page 280)
Initial direction in up-down-count mode.

Initial State (see page 287)
Initial output state for ST.

Probe Signals

CC4yPRS
Period Register.

CC4yCRS
Compare Register.

CC4yPSL
Passive Level Register status.

CC4x.INyAA
AA Input Signal status.

CC4x.INyAB
AB Input Signal status.

CC4x.INyAC
AC Input Signal status.

CC4x.INyAD
AD Input Signal status.

CC4xSTy
Status bit.

CC4xOUTy
Output status.

CC4yINTS
Interrupt Status Register status.

CC4yPSC
Prescaler Register status.

CC4yINS1
Input Selector Register 1 status.

CC4yINS2
Input Selector Register 2 status.

CC4yINTE
Interrupt Enable Register status.

CC4yCMC
Connection Matrix Control Register status.

CC4yTC
Slice Timer Control Register status.

CC4ySTC
Shadow Transfer Control Register status.

FLAGS
Flags for further system analysis (see page 289).

Infineon XMC1000 CCU8 Slice Compare Mode GUI

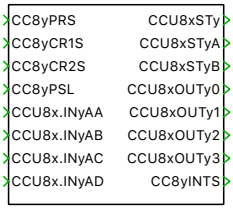
Purpose

High fidelity model of a Infineon CCU8 Timer slice with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / Infineon XMC1000 / CCU

Description



This block efficiently models the behavior of a single Infineon XMC1000 CCU8 timer slice with full timing resolution. The component is focused to the capture mode. Beneath the typical PWM generation it also supports the external override, trap and modulation features. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the Infineon XMC1000 CCU8 timer slice. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “CCU8 Single Timer Slice (Compare Mode)” (on page 290).

Parameters

General

MCLK [Hz] (see page 291)
The base clock of the CCU8 defined in Hz.

CC8yPSC (see page 291)
Defines a clock prescaler.

CC8yTC.TCM (see page 291)
Defines the counter mode.

CC8yTC.TRAPEx (see page 302)
Enables trap functionality for output channel x.

CC8yTC.TRAPSE (see page 302)
Defines trap release behavior.

CC8yTC.EMS (see page 302)
Defines the modulation synchronization behavior.

CC8yTC.EMT (see page 302)
Defines the modulation behavior.

CC8yTC.EME (see page 302)
Configures compare channels affected by the modulation feature.

CC8yTC.STOS (see page 302)
Defines to which channel *CC8ySTy* is mapped.

CC8ySTC.STM (see page 291)
Defines the shadow transfer events in center aligned mode.

Initial Counter (see page 291)
Counter initialization.

Initial Direction (see page 291)
Initial direction in up-down-count mode.

Initial STx State (see page 302)
Initial STx state.

Input Selection

CC8yINS1.EVxIS (see page 298)
Specifies input source for event x.

CC8yINS2.EVxEM (see page 298)
Specifies edges used as trigger for event x.

CC8yINS2.EVxLM (see page 298)
Specifies level used for event x.

Connection Matrix

CC8yCMC.OFS (see page 300)
Enables and connects override functionality.

CC8yCMC.TS (see page 300)
Enables and connects trap functionality.

CC8yCMC.MOS (see page 300)
Connects modulation functionality to an event.

Channel Control

CC8yCHC.ASE (see page 291)
Defines status bit generation mode.

CC8yCHC.OCSx (see page 302)
Define status bit to output x mapping.

Dead Time

CC8yDTC.DTEx (see page 296)
Enables deadtime feature for compare channel x.

CC8yDTC.DCENx (see page 296)
Enables deadtime feature for related status bit.

CC8yDTC.DTCC (see page 296)
Defines clock prescaling for deadtime counters.

CC8yDTC.DTxR (see page 296)
Defines delay for positive edge of STx.

CC8yDTC.DTxF (see page 296)
Defines delay for positive edge of inverted STx.

Interrupt Enable

CC8yINTE.PME (see page 306)
Enables interrupt for period match event.

CC8yINTE.OME (see page 306)
Enables interrupt for one match event.

CC8yINTE.CMU1E (see page 306)
Enables interrupt for compare match 1 event while upcounting.

CC8yINTE.CMD1E (see page 306)
Enables interrupt for compare match 1 event while downcounting.

CC8yINTE.CMU2E (see page 306)
Enables interrupt for compare match 2 event while upcounting.

CC8yINTE.CMD2E (see page 306)
Enables interrupt for compare match 2 event while downcounting.

CC8yINTE.ExAE (see page 306)
Enables interrupt for event x detection.

Probe Signals

CC8yPRS
Period Register.

CC8yCR1S
Compare Register.

CC8yCR2S
Compare Register.

CC8yPSL
Passive Level Register status.

CC8x.INyAA
AA Input Signal status.

CC8x.INyAB
AB Input Signal status.

CC8x.INyAC
AC Input Signal status.

CC8x.INyAD
AD Input Signal status.

CC8xSTy
Status bit output y.

CC8xSTA
Status bit output A.

CC8xSTB
Status bit output B.

CC8xOUT0
Output status 0.

CC8xOUT1
Output status 1.

CC8xOUT2
Output status 2.

CC8xOUT3
Output status 3.

CC8yINTS
Interrupt Status Register status.

CC8yPSC
Prescaler Register status.

CC8yINS1
Input Selector Register 1 status.

CC8yINS2
Input Selector Register 2 status.

CC8yINTE
Interrupt Enable Register status.

CC8yCMC
Connection Matrix Control Register status.

CC8yTC
Slice Timer Control Register status.

CC8ySTC
Shadow Transfer Control Register status.

CC8yCHC
Channel Control Register status.

CC8yDTC
Dead Time Control Register status.

CC8yDCxR
Channel x Dead Time Counter Values status.

FLAGS
Flags for further system analysis (see page 306).

Infineon XMC1000 CCU8 Slice Compare Mode REG

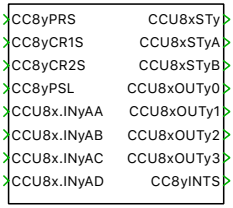
Purpose

High fidelity model of a Infineon CCU8 Timer slice with register based configuration.

Library

Processor in the Loop / Peripherals / Infineon XMC1000 / CCU

Description



This block efficiently models the behavior of a single Infineon XMC1000 CCU8 timer slice with full timing resolution. The component is focused to the capture mode. Beneath the typical PWM generation it also supports the external override, trap and modulation features. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “CCU8 Single Timer Slice (Compare Mode)” (on page 290).

Parameters

MCLK [Hz] (see page 291)
The base clock of the CCU8 defined in Hz.

CC8yPSC (see page 291)
Defines a clock prescaler.

CC8yTC (see page 302)
Slice Timer Control Register.

CC8yINS1 (see page 298)
Input Selector Register 1.

CC8yINS2 (see page 298)
Input Selector Register 2.

CC8yCMC (see page 300)
Connection Matrix Control Register.

CC8yINTE (see page 306)
Interrupt Enable Register.

CC8ySTC (see page 291)
Shadow Transfer Control Register.

CC8yCHC (see page 302)
Shadow Transfer Control Register.

CC8yDTC (see page 296)
Dead Time Control Register.

CC8yDCxR (see page 296)
Channel x Dead Time Counter Values Register.

Initial Counter (see page 291)
Counter initialization.

Initial Direction (see page 291)
Initial direction in up-down-count mode.

Initial STx State (see page 302)
Initial STx state.

Probe Signals

CC8yPRS
Period Register.

CC8yCR1S
Compare Register.

CC8yCR2S
Compare Register.

CC8yPSL
Passive Level Register status.

CC8x.INyAA
AA Input Signal status.

CC8x.INyAB
AB Input Signal status.

CC8x.INyAC
AC Input Signal status.

CC8x.INyAD
AD Input Signal status.

CC8xSTy
Status bit output y.

CC8xSTA
Status bit output A.

CC8xSTB
Status bit output B.

CC8xOUT0
Output status 0.

CC8xOUT1
Output status 1.

CC8xOUT2
Output status 2.

CC8xOUT3
Output status 3.

CC8yINTS
Interrupt Status Register status.

CC8yPSC
Prescaler Register status.

CC8yINS1
Input Selector Register 1 status.

CC8yINS2
Input Selector Register 2 status.

CC8yINTE
Interrupt Enable Register status.

CC8yCMC
Connection Matrix Control Register status.

CC8yTC
Slice Timer Control Register status.

CC8ySTC
Shadow Transfer Control Register status.

CC8yCHC
Channel Control Register status.

CC8yDTC
Dead Time Control Register status.

CC8yDCxR
Channel x Dead Time Counter Values status.

FLAGS
Flags for further system analysis (see page 306).

TI C2000 ADC Type 2 GUI

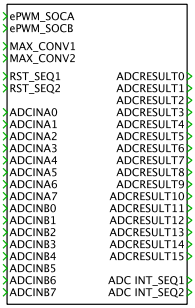
Purpose

High fidelity model of TI's C2000 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 2 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 2 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 2" (on page 74).

Parameters

ADC General

HSPCLK [Hz] (see page 76)
The system clock of the processor defined in Hz.

ADCTRL3.ADCCLKPS (see page 76)
Register cell defining a clock prescaler.

ADCTRL1.CPS (see page 76)
Register cell defining a clock prescaler.

Vref [VREFLO, VREFH] (see page 75)
Specification of reference voltage in mask.

ADCTRL1.ACQ_PS (see page 76)
Specification the width of the ADC sampling window.

Output Mode (see page 76)
Defines representation of conversion results.

Sequencer x Reset (see page 78)
Determines reset of Sequencer x state-pointer either internally after an EOS event or externally through the RST_SEQx input.

ADCTRL

ADCTRL1.SEQ_CASC (see page 78)
Selects operation of ADC in Dual or Cascaded sequencing mode.

ADCTRL2.ePWM_SOCy_SEQx (see page 80)
Enables the start-of-conversion of SEQx by a ePWM_SOCy trigger.

ADCTRL2.INT_MOD_SEQx (see page 80)
Selects the generation of an ADC interrupt at every EOS or every other EOS for SEQx.

ADCTRL2.INT_ENA_SEQx (see page 80)
Enables the generation of an ADC interrupt for SEQx.

ADCTRL2.ePWM_SOCB_SEQ (see page 80)
Enables the start-of-conversion of SEQ by a ePWM_SOCB trigger.

ADCTRL3.SMODE_SEL (see page 80)
Selects the operation of the ADC in simultaneous or sequential sampling mode.

ADCCHSELSEQx

CONVnn (see page 78)
Selects input channel converted by the ADC.

Probe Signals

Pending SEQx Trigger
Pending trigger for SEQx.

SOC Flag
Start of conversion flag for ADC.

EOS Flag for SEQx
Generates an end-of-sequence signal for SEQx.

ADCCTLx
ADC Control registers resulting from mask settings.

ADCMAXCONV
Maximum ADC conversions resulting from MAX_CONV1 and MAX_CONV2 inputs.

ADCCHSELSEQx
ADC Channel select resulting from mask settings.

TI C2000 ADC Type 2 REG

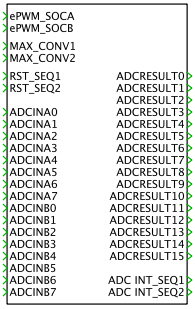
Purpose

High fidelity model of TI's C2000 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 2 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 2" (on page 74).

Parameters

HSPCLK [Hz] (see page 76)
The system clock of the processor defined in Hz.

Vref [VREFLO, VREFH] (see page 76)
Specification of reference voltage in mask.

ADCTRLx (see page 78)
ADC Control register x.

ADCCHSELSEQx (see page 78)
ADC Channel select register x.

Output Mode (see page 76)
Defines representation of conversion results.

Sequencer x Reset (see page 78)
Determines reset of Sequencer x state-pointer either internally after an EOS event or externally through the RST_SEQx input.

Probe Signals

Pending SEQx Trigger
Pending trigger for SEQx.

SOC Flag
Start of conversion flag for ADC.

EOS Flag for SEQx
Generates an end-of-sequence signal for SEQx.

ADCCTLx
ADC Control registers resulting from mask settings.

ADCMAXCONV
Maximum ADC conversions resulting from MAX_CONV1 and MAX_CONV2 inputs.

ADCCHSELSEQx
ADC Channel select resulting from mask settings.

TI C2000 ADC Type 3 GUI

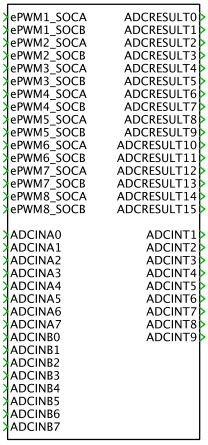
Purpose

High fidelity model of TI's C2000 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 3 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 3 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 3" (on page 83).

Parameters

ADC General

System Clock [Hz] (see page 85)
The system clock of the processor defined in Hz.

ADCCTL2.CLKDIV4EN (see page 85)
Register cell defining a clock prescaler.

ADCCTL2.CLKDIV2EN (see page 85)
Register cell defining a clock prescaler.

ADCCTL1.ADCREFSEL (see page 85)
Register cell choosing the reference voltage.

External Reference [LO,HI] (see page 85)
Specification of external reference voltage in mask.

ADCCTL1.INTPULSEPOS (see page 90)
Defines position of EOC and interrupt flags.

ADCCTL1.ADCNONOVERLAP (see page 85)
Allows/Inhibits overlap of conversion and sampling.

Output Mode (see page 85)
Defines representation of conversion results.

ADC INTSELxNy

INTSELxNy.INTxE (see page 90)
Enables interrupt generation for INTx.

INTSELxNy.INTxSEL (see page 90)
Defines trigger (EOC flag) for INTx.

ADCSOCx/y

ADCSOCxCTL.TRIGSEL (see page 86)
Defines trigger source for SOCx.

ADCINTSOCSEL1.SOCx (see page 90)
Defines SOCx trigger to be an interrupt. Overwrites TRIGSEL selection if not chosen to NO ADCINT.

ADCSOCxCTL.CHSEL (see page 86)
Selects input channel converted by SOCx.

ADCSOCxCTL.ACQPS (see page 86)
Defines length of sampling window for SOCx.

ADCSAMPLEMODE.SIMULENx (see page 89)
Defines sample mode for SOCx/SOCx+1 pair.

Probe Signals

ADCCTLx
ADC Control registers resulting from mask settings.

ADCSAMPLEMODE
Sample mode control register resulting from mask settings.

ADCSOCxCTL
ADC SOC control registers resulting from mask settings.

INTSELxNy
ADC interrupt module control registers resulting from mask settings.

ADCINTSOCSELx
ADC SOC interrupt trigger control registers resulting from mask settings.

TI C2000 ADC Type 3 REG

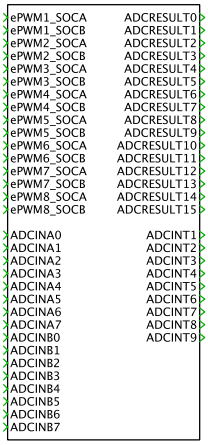
Purpose

High fidelity model of TI's C2000 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 3 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 3" (on page 83).

Parameters

System Clock [Hz] (see page 85)
The system clock of the processor defined in Hz.

ADCCTL1 (see page 85)
ADC Control register 1.

ADCCTL2 (see page 85)
ADC Control register 2.

External Reference [LO,HI] (see page 85)
Specification of external reference voltage in mask.

ADCSAMPLEMODE (see page 89)
Sample mode control registers for SOC pairs.

ADCSOCxCTL (see page 86)
ADC SOC control register for SOCx.

INTSELxNy (see page 90)
ADC interrupt module control registers.

ADCINTSOCSELx (see page 90)
ADC SOC interrupt trigger control registers.

Output Mode (see page 85)
Defines representation of conversion results.

Probe Signals

ADCCTLx
ADC control registers.

ADCSAMPLEMODE
Sample mode Control register.

ADCSOCxCTL
ADC SOC control registers.

INTSELxNy
ADC interrupt module control registers.

ADCINTSOCSELx
ADC SOC interrupt trigger control registers.

TI C2000 ADC Type 3 Simplified

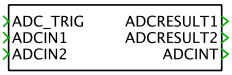
Purpose

Simplified model of TI's C2000 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block provides a simplified model of the TI Type 3 ADC module retaining the timing behavior of the hardware ADC. The component supports either single or simultaneous measurements with configurable sample window length and conversion voltage reference. Due to simulation efficiency reasons, the conversion results are calculated as the average of the input values at the begin and the end of the sampling window. The component further provides an interrupt pulse on the output which indicates an available conversion result.

In single sampling mode, a pulse on the trigger input invokes a single conversion of *ADCIN1*. The *ADCINT* pulse indicates that the conversion result is available at *ADCRESULT1*.

In simultaneous sampling mode, *ADCIN1* and *ADCIN2* are sampled simultaneously. The *ADCINT* pulse indicates that the conversion result is available at *ADCRESULT1* and *ADCRESULT2*.

Parameters

ADC clock [Hz]
The ADC time base clock defined in Hz.

Sampling Mode
Defines sampling mode of ADC.

Sample Window length
Defines length of sampling window based on the adc clock period.

Reference Selection
Defines reference voltage range used for conversion.

External Reference [LO,HI]
Specification of external reference voltage in mask.

Output Mode
Defines representation of conversion results.

Probe Signals

ADC_Trig
Trigger input of simplified ADC.

ADCINx
Measurement inputs of simplified ADC.

ADCRESULTx
Conversion results of simplified ADC.

ADCINT
Conversion result available pulse of simplified ADC.

TI C2000 ADC Type 4 GUI

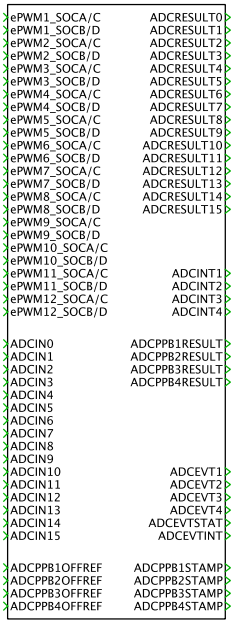
Purpose

High fidelity model of TI's C2000 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 4 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 4 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 4" (on page 92).

Parameters

ADC General

System Clock [Hz] (see page 94)
The system clock of the processor defined in Hz.

ADCCTL2.PRESCALE (see page 94)
Register cell defining the ADC clock based on the System Clock.

ADCCTL2.SIGNALMODE (see page 94)
Register cell defining the mode and resolution used for conversion.

Voltage Reference [LO,HI] (see page 99)
Specification of external reference voltage in mask.

Output Mode (see page 94)
Defines representation of conversion results.

ADC INTSELxNy

ADCINTSELxNy.INTxE (see page 100)
Enables interrupt generation for INTx.

ADCINTSELxNy.INTxSEL (see page 100)
Defines trigger (EOC flag) for INTx.

ADCSOCx/y

ADCSOCxCTL.TRIGSEL (see page 96)
Defines trigger source for SOCx.

ADCINTSOCSEL1.SOCx (see page 100)
Defines SOCx trigger to be an interrupt. Overwrites TRIGSEL selection if not chosen to NO ADCINT.

ADCSOCxCTL.CHSEL (see page 96)
Selects input channel converted by SOCx.

ADCSOCxCTL.ACQPS (see page 96)
Defines length of sampling window for SOCx.

PPBx

ADCPPBxCONFIG.CONFIG (see page 102)
Defines associated SOC.

ADCPPBxCONFIG.TWOSCOMPEN (see page 102)
Enables inversion of error calculation.

ADCEVTSEL.PPBxZERO (see page 102)
Enables event generation for ADCPPBxRESULT zero crossing detection.

ADCEVTSEL.PPBxTRIPLO (see page 102)
Enables event generation for ADCPPBxRESULT low level limit detection.

ADCEVTSEL.PPBxTRIPHI (see page 102)
Enables event generation for ADCPPBxRESULT high level limit detection.

ADCEVTINTSEL.PPBxZERO (see page 102)
Enables interrupt for ADCPPBxRESULT zero crossing detection.

ADCEVTINTSEL.PPBxTRIPLO (see page 102)
Enables interrupt for ADCPPBxRESULT low level limit detection.

ADCEVTINTSEL.PPBxTRIPHI (see page 102)
Enables interrupt for ADCPPBxRESULT high level limit detection.

ADCPPBxOFFSET (see page 102)
Defines ADCRESULTx offset.

ADCPPBxTRIPHI (see page 102)
Defines ADCPPBxRESULT high level limit.

ADCPPBxTRIPLO (see page 102)
Defines ADCPPBxRESULT low level limit.

Probe Signals

ADCCTLx
ADC Control registers resulting from mask settings.

ADCSOCxCTL
ADC SOC control registers resulting from mask settings.

ADCINTSELxNy
ADC interrupt module control registers resulting from mask settings.

ADCINTSOCSELx
ADC SOC interrupt trigger control registers resulting from mask settings.

ADCEVTSEL
Configuration register for PPBx event generation.

ADCEVTINTSEL
Configuration register for PPBx interrupt generation.

ADCPPBxCONFIG
Configuration register for PPBx.

ADCPPBxOFFCAL
ADCPPBx offset register.

ADCPPBxTRIPHI
ADCPPBx high level trip register.

ADCPPBxTRIPLO
ADCPPBx low level trip register.

TI C2000 ADC Type 4 REG

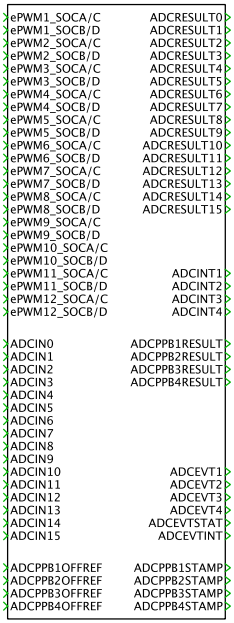
Purpose

High fidelity model of TI's C2000 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ADC

Description



This block models the TI Type 4 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Analog Digital Converter (ADC) Type 4" (on page 92).

Parameters

ADC

System Clock [Hz] (see page 94)
The system clock of the processor defined in Hz.

ADCCTL1 (see page 100)
ADC Control register 1.

ADCCTL2 (see page 94)
ADC Control register 2.

Voltage Reference [LO,HI] (see page 99)
Specification of external reference voltage in mask.

ADCSOCxCTL (see page 96)
ADC SOC control register for SOCx.

ADCINTSELxNy (see page 100)
ADC interrupt module control registers.

ADCINTSOCSELx (see page 100)
ADC SOC interrupt trigger control registers.

Output Mode (see page 94)
Defines representation of conversion results.

PPB

ADCEVTSEL (see page 102)
Configuration register for PPBx event generation.

ADCEVTINTSEL (see page 102)
Configuration register for PPBx interrupt generation.

ADCPPBxCONFIG (see page 102)
Configuration register for PPBx.

ADCPPBxOFFCAL (see page 102)
ADCPPBx offset register.

ADCPPBxTRIPHI (see page 102)
ADCPPBx high level trip register.

ADCPPBxTRIPLO (see page 102)
ADCPPBx low level trip register.

Probe Signals

ADCCTLx
ADC control registers.

ADCSOCxCTL
ADC SOC control registers.

ADCINTSELxNy
ADC interrupt module control registers.

ADCINTSOCSELx
ADC SOC interrupt trigger control registers.

ADCEVTSEL
Configuration register for PPBx event generation.

ADCEVTINTSEL
Configuration register for PPBx interrupt generation.

ADCPPBxCONFIG
Configuration register for PPBx.

ADCPPBxOFFCAL
ADCPPBx offset register.

ADCPPBxTRIPHI
ADCPPBx high level trip register.

ADCPPBxTRIPLO
ADCPPBx low level trip register.

TI C2000 eCAP Type 0 APWM GUI

Purpose

High fidelity model of TI's C2000 eCAP module operated in APWM mode with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / eCAP

Description

This block efficiently models the behavior of a single TI Type 0 eCAP module operated in APWM mode. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Capture (eCAP) Module Type 0" (on page 107).

Parameters

System Clock [Hz] (see page 110)
The system clock of the processor defined in Hz.

Counter Sampling Frequency [Hz] (see page 111)
Frequency at which the counter value is updated.

ECCTL2.APWMPOL (see page 110)
Select output of APWM module to be active high or low.

ECEINT.CTR=CMP (see page 110)
Enable interrupt generation at compare event.

ECEINT.CTR=PRD (see page 110)
Enable generation of interrupt at period event.

ECEINT.CTROVF (see page 110)
Enable generation of interrupt at counter overflow event.

Probe Signals

CAPx register
Capture x register.

eCAP Counter
Counter value sampled at user specified frequency

TI C2000 eCAP Type 0 CAP GUI

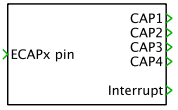
Purpose

High fidelity model of TI's C2000 eCAP module operated in Capture mode with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / eCAP

Description



This block efficiently models the behavior of a single TI Type 0 eCAP module operated in capture mode. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 0 eCAP module operated in capture mode. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Capture (eCAP) Module Type 0" (on page 107).

Parameters

eCAP General

System Clock [Hz] (see page 108)
The system clock of the processor defined in Hz.

Counter Sampling Frequency [Hz] (see page 111)
Frequency at which the counter value is updated.

ECCTL1

ECCTL1.CAPxPOL (see page 109)
Select CAPx capture events on rising or falling edge.

ECCTL1.CTRSTx (see page 109)
Enable counter reset after CAPx capture event.

ECCTL1.CAPLDEN (see page 109)
Enable loading of counter value into capture registers on capture events.

ECCTL1.PRESCALE (see page 108)
Event prescaler bits to reduce the frequency of the input capture signal.

ECCTL2

ECCTL2.STOP_WRAP (see page 109)
Select capture event after which counter wrapping occurs.

ECEINT

ECEINT.CEVTx (see page 110)
Enable interrupt generation at capture event x.

ECEINT.CTROVF (see page 110)
Enable generation of interrupt at counter overflow event.

Probe Signals

eCAP PSout
Post-scaled ECAPx pin events.

eCAP Counter
Counter value sampled at user specified frequency.

ECCTLx
ECAP control register x.

ECEINT
ECAP interrupt enable register.

TI C2000 eCAP Type 0 CAP REG

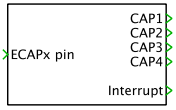
Purpose

High fidelity model of TI's C2000 eCAP module operated in capture mode with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / eCAP

Description



This block efficiently models the behavior of a single TI Type 0 eCAP module operated in capture mode. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Capture (eCAP) Module Type 0" (on page 107).

Parameters

System Clock [Hz] (see page 108)
The system clock of the processor defined in Hz.

Counter Sampling Frequency [Hz] (see page 111)
Frequency at which the counter value is updated.

ECCTLx (see page 108)
ECAP control register x.

ECEINT (see page 108)
ECAP interrupt enable register.

Probe Signals

eCAP PSout
Post-scaled ECAPx pin events.

eCAP Counter
Counter value sampled at user specified frequency.

ECCTLx
ECAP control register x.

ECEINT
ECAP interrupt enable register.

TI C2000 ePWM Type 1 Configurator

Purpose

Helper block for generation of AQCTLx and AQCSFRC registers

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description

This block generates the decimal value for the Action-Qualifier Control Register (AQCTLx) and the Action-Qualifier Continuos Software Force Register (AQCSFRC) based on the configuration of the mask parameters.

Parameters

AQCTLA

Action-Qualifier Output A Control Register Filed Descriptions

AQCTLA.CBD
Action when the TB-counter equals the active CMPB register and the counter is decrementing.

AQCTLA.CBU
Action when the TB-counter equals the active CMPB register and the counter is incrementing.

AQCTLA.CAD
Action when the TB-counter equals the active CMPA register and the counter is decrementing.

AQCTLA.CAU
Action when the TB-counter equals the active CMPA register and the counter is incrementing.

AQCTLA.PRD
Action when the TB-counter equals the period.

AQCTLA.ZRO
Action when the TB-counter equals zero.

AQCTLB

Action-Qualifier Output B Control Register Filed Descriptions

AQCTLB.CBD
Action when the TB-counter equals the active CMPB register and the counter is decrementing.

AQCTLB.CBU
Action when the TB-counter equals the active CMPB register and the counter is incrementing.

AQCTLB.CAD
Action when the TB-counter equals the active CMPA register and the counter is decrementing.

AQCTLB.CAU
Action when the TB-counter equals the active CMPA register and the counter is incrementing.

AQCTLB.PRD
Action when the TB-counter equals the period.

AQCTLB.ZRO
Action when the TB-counter equals zero.

AQSRFC

Action-Qualifier Continuos Software Force Register Field Descriptions

AQSRFC.CSFD
Continuous Software Force on Output B.

AQSRFC.CSFA
Continuous Software Force on Output A.

TI C2000 ePWM Type 1 GUI

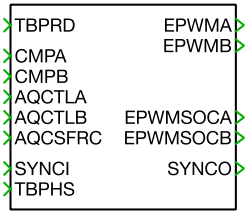
Purpose

High fidelity model of TI's C2000 ePWM module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description



This block efficiently models the behavior of a single TI Type 1 ePWM module with full timing resolution for a variable PWM period. Beneath the typical PWM generation it also supports the features provided by the Event Trigger and the Deadband submodule. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 1 ePWM module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Pulse Width Modulator (ePWM) Type 1" (on page 43).

Parameters

ePWM General

System Clock [Hz] (see page 45)
The system clock of the processor defined in Hz.

TBCTL.PHSDIR (see page 46)
Register cell defining the counter direction after a synch event.

TBCTL.CLKDIV (see page 45)
Register cell defining a clock prescaler.

TBCTL.HSPCLKDIV (see page 45)
Register cell defining a high speed clock prescaler.

TBCTL.SYNCOSEL (see page 46)
Register cell defining SYNCO behavior.

TBCTL.PHSEN (see page 46)
Register cell enabling counter synchronization.

TBCTL.CTRMODE (see page 45)
Register cell for count mode configuration.

CMPCTL.LOADxMODE (see page 48)
Specification of Reload Event for CMPx.

AQSFRC.RLDCSF (see page 49)
Specification of Reload Event for AQCSFRC.

Initial Counter (see page 46)
Counter initialization.

Initial Direction (see page 46)
Initial direction in up-down-count mode.

Initial State (see page 46)
Initial output state for EPWMA and EPWMB.

Event-Trigger module

ETSEL.SOCxEN (see page 53)
Enables pulse generation on EPWMSOCx.

ETSEL.SOCxSEL (see page 53)
Selects event source for Event-Trigger counter increment.

ETSEL.SOCxCNT (see page 53)
Sets initial Event-Trigger counter value.

ETSEL.SOCxPRD (see page 53)
Specifies Event-Trigger counter period.

Dead-Band module

DBCTL.HALFCYCLE (see page 55)
Enables clocking of DB-counter with halfed time-base period.

DBCTL.INMODE (see page 55)
Configures input source to the falling-edge and rising-edge delays.

DBCTL.POLSEL (see page 55)
Specifies polarity inversion of the edge delay outputs.

DBCTL.OUTMODE (see page 55)
Selectively enable or bypass the Dead-Band generation.

DBCTL.DBRED (see page 55)
Dead-Band generator rising-edge delay.

DBCTL.DBFED (see page 55)
Dead-Band generator falling-edge delay.

Probe Signals

CMPx
Compare register.

AQCTLx
Action qualifier configuration.

AQCSFRC
Action qualifier software forcing configuration.

EPWMx
EPWM outputs.

EPWMSOCx
EPWM SOC pulse outputs.

TBPRD
Period of PWM counter.

TBCTL
Time-Base control register resulting from mask settings.

CMPCTL
Compare-Control register resulting from mask settings.

AQSFRC
Action-Qualifier software force register resulting from mask settings.

ETSEL
Event-Trigger selection register resulting from mask settings.

ETPS
Event-Trigger prescale register resulting from mask settings.

DBCTL
Dead-Band control register resulting from mask settings.

DBRED
Dead-Band generator rising-edge delay register resulting from mask settings.

DBRED
Dead-Band generator falling-edge delay register resulting from mask settings.

SYNCI
Synchronization input.

TBPHS
Synchronization value.

SYNCO
Synchronization output.

FLAGS
Counter value, event flags and counting direction.

TI C2000 ePWM Type 1 REG

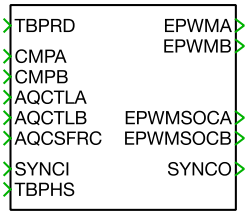
Purpose

High fidelity model of TI's C2000 ePWM module with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description



This block efficiently models the behavior of a single TI Type 1 ePWM module with full timing resolution for a variable PWM period. Beneath the typical PWM generation it also supports the features provided by the Event Trigger and the Deadband submodule. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Pulse Width Modulator (ePWM) Type 1" (on page 43).

Parameters

System Clock [Hz] (see page 45)
The system clock of the processor defined in Hz.

TBPRD (see page 45)
Period value of the internal counter defining the period of the PWM signal.

TBCTL (see page 45)
Time-Base control register.

CMPCTL (see page 48)
Compare control register.

AQSFRC (see page 49)
Action-Qualifier software force register.

ETSEL (see page 53)
Event-Trigger selection register.

ETPS (see page 53)
Event-Trigger prescale register.

DBCTL (see page 55)
Dead-Band control register.

DBRED (see page 55)
Dead-Band generator rising-edge delay register.

DBRED (see page 55)
Dead-Band generator falling-edge delay register.

Initial Counter (see page 46)
Counter initialization.

Initial Direction (see page 46)
Initial direction in up-down-count mode.

Initial State (see page 46)
Initial output state for EPWMA and EPWMB.

Probe Signals

CMPx
Compare register.

AQCTLx
Action qualifier configuration.

AQCSFRC
Action qualifier software forcing configuration.

EPWMx
EPWM outputs.

EPWMSOCx
EPWM SOC pulse outputs.

TBPRD
Period of PWM counter.

TBCTL
Time-Base control register.

CMPCTL
Compare-Control register.

AQSFRC
Action-Qualifier software force register.

ETSEL
Event-Trigger selection register.

ETPS
Event-Trigger prescale register.

DBCTL
Dead-Band control register.

DBRED
Dead-Band generator rising-edge delay register.

DBRED
Dead-Band generator falling-edge delay register.

SYNCI
Synchronization input.

TBPHS
Synchronization value.

SYNCO
Synchronization output.

FLAGS
Counter value, event flags and counting direction.

TI C2000 ePWM Type 4 Configurator

Purpose

Helper block for generation of AQCTLx, AQCTLx2, and AQCSFRC registers

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description

This block generates the decimal value for the Action-Qualifier Control Register (AQCTLx), Action-Qualifier Control Register 2 (AQCTLx2) and the Action-Qualifier Continuos Software Force Register (AQCSFRC) based on the configuration of the mask parameters.

Parameters

AQCTLA

Action-Qualifier Output A Control Register Filed Descriptions

AQCTLA.CBD
Action when the TB-counter equals the active CMPB register and the counter is decrementing.

AQCTLA.CBU
Action when the TB-counter equals the active CMPB register and the counter is incrementing.

AQCTLA.CAD
Action when the TB-counter equals the active CMPA register and the counter is decrementing.

AQCTLA.CAU
Action when the TB-counter equals the active CMPA register and the counter is incrementing.

AQCTLA.PRD
Action when the TB-counter equals the period.

AQCTLA.ZRO
Action when the TB-counter equals zero.

AQCTLA2

Action-Qualifier Output A Control Register 2 Filed Descriptions

AQCTLA2.T2D
Action when T2 event occurs and the counter is decrementing.

AQCTLA2.T2U
Action when T2 event occurs and the counter is incrementing.

AQCTLA2.T1D
Action when T1 event occurs and the counter is decrementing.

AQCTLA2.T1U
Action when T1 event occurs and the counter is incrementing.

AQCTLB

Action-Qualifier Output B Control Register Filed Descriptions

AQCTLB.CBD
Action when the TB-counter equals the active CMPB register and the counter is decrementing.

AQCTLB.CBU
Action when the TB-counter equals the active CMPB register and the counter is incrementing.

AQCTLB.CAD
Action when the TB-counter equals the active CMPA register and the counter is decrementing.

AQCTLB.CAU
Action when the TB-counter equals the active CMPA register and the counter is incrementing.

AQCTLB.PRD
Action when the TB-counter equals the period.

AQCTLB.ZRO
Action when the TB-counter equals zero.

AQCTLB2

Action-Qualifier Output B Control Register 2 Filed Descriptions

AQCTLB2.T2D
Action when T2 event occurs and the counter is decrementing.

AQCTLB2.T2U
Action when T2 event occurs and the counter is incrementing.

AQCTLB2.T1D
Action when T1 event occurs and the counter is decrementing.

AQCTLB2.T1U
Action when T1 event occurs and the counter is incrementing.

AQSRFC

Action-Qualifier Continuos Software Force Register Field Descriptions

AQSRFC.CSFD
Continuous Software Force on Output B.

AQSRFC.CSFA
Continuous Software Force on Output A.

TI C2000 ePWM Type 4 GUI

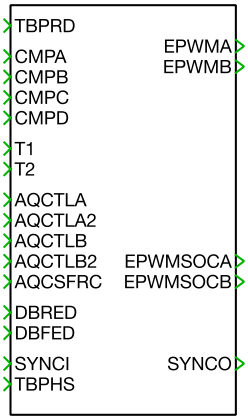
Purpose

High fidelity model of TI's C2000 ePWM module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description



This block efficiently models the behavior of a single TI Type 4 ePWM module with full timing resolution for a variable PWM period. Beneath the typical PWM generation it also supports the features provided by the Event Trigger and the Deadband submodule. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 4 ePWM module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Pulse Width Modulator (ePWM) Type 4" (on page 57).

Parameters

ePWM General

System Clock [Hz] (see page 59)
The system clock of the processor defined in Hz.

EPWMCLK Prescaler (see page 59)
Prescaler to divide down the system clock to generate the EPWM clock.

TBCTL.PHSDIR (see page 60)
Register cell defining the counter direction after a synch event.

TBCTL.CLKDIV (see page 59)
Register cell defining a clock prescaler.

TBCTL.HSPCLKDIV (see page 59)
Register cell defining a high speed clock prescaler.

TBCTL.SYNCOSEL (see page 60)
Register cell defining SYNCO behavior.

TBCTL.PHSEN (see page 60)
Register cell enabling counter synchronization.

TBCTL.CTRMODE (see page 59)
Register cell for count mode configuration.

TBCTL2.PRDLDSYNC (see page 60)
Register cell defining the period reload behavior for synch events.

TBCTL2.SYNCOSELX (see page 60)
Register cell defining SYNCO behavior.

CMPCTL.LOADxMODE (see page 63)
Specification of Reload Event for CMPx.

AQSFRC.RLDCSF (see page 64)
Specification of Reload Event for AQCSFRC.

Initial Counter (see page 60)
Counter initialization.

Initial Direction (see page 60)
Initial direction in up-down-count mode.

Initial State (see page 60)
Initial output state for EPWMA and EPWMB.

Event-Trigger module

ETSEL.SOCxEN (see page 68)
Enables pulse generation on EPWMSOCx.

ETSEL.SOCxSEL (see page 68)
Selects event source for Event-Trigger counter increment.

ETSEL.SOCxSELCMP (see page 68)
Selects CMPA/CMPB or CMPC/CMPD as event source for Event-Trigger counter increment.

ETPS.SOCxPRD (see page 68)
Specifies Event-Trigger 2-bit counter period.

ETPS.SOCPSSEL (see page 68)
Selects ETPS[SOCxPRD] or ETSOCPS[SOCxPRD2] to determine frequency of events

ETSOCPS.SOCxPRD2 (see page 68)
Specifies Event-Trigger 4-bit counter period.

ETCNTINIT.SOCxINIT (see page 68)
Sets initial Event-Trigger counter value.

Dead-Band module

DBCTL.HALFCYCLE (see page 71)
Enables clocking of DB-counter with halfed time-base period.

DBCTL.DEDB_MODE (see page 71)
Enables dual edge dead-band mode.

DBCTL.OUTSWAP (see page 71)
Swaps one or both output signals.

DBCTL.LOADFEDMODE (see page 71)
Controls transfer of DBFED shadow to active register.

DBCTL.LOADREDMODE (see page 71)
Controls transfer of DBRED shadow to active register.

DBCTL.INMODE (see page 71)
Configures input source to the falling-edge and rising-edge delays.

DBCTL.POLSEL (see page 71)
Specifies polarity inversion of the edge delay outputs.

DBCTL.OUTMODE (see page 71)
Selectively enable or bypass the Dead-Band generation.

Probe Signals

CMPx
Compare register.

Tx
Tx events.

AQCTLx
Action qualifier configuration.

AQCTLx2
Action qualifier configuration.

AQCSFRC
Action qualifier software forcing configuration.

EPWMx
EPWM outputs.

EPWMSOCx
EPWM SOC pulse outputs.

TBPRD
Period of PWM counter.

TBCTL
Time-Base control register resulting from mask settings.

TBCTL2
Time-Base control register 2.

CMPCTL
Compare-Control register resulting from mask settings.

CMPCTL2
Compare-Control register 2 resulting from mask settings.

AQSFRC
Action-Qualifier software force register resulting from mask settings.

ETSEL
Event-Trigger selection register resulting from mask settings.

ETPS
Event-Trigger prescale register resulting from mask settings.

ETCNTINIT
Event-Trigger counter initialization register resulting from mask settings.

ETSOCPS
Event-Trigger SOC prescaler register resulting from mask settings.

DBCTL
Dead-Band control register resulting from mask settings.

DBRED
Dead-Band generator rising-edge delay register.

DBRED
Dead-Band generator falling-edge delay register.

SYNCI
Synchronization input.

TBPHS
Synchronization value.

SYNCO
Synchronization output.

FLAGS
Counter value, event flags and counting direction.

TI C2000 ePWM Type 4 REG

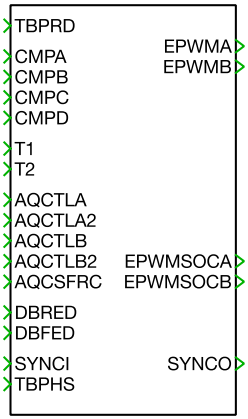
Purpose

High fidelity model of TI's C2000 ePWM module with register based configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / ePWM

Description



This block efficiently models the behavior of a single TI Type 4 ePWM module with full timing resolution for a variable PWM period. Beneath the typical PWM generation it also supports the features provided by the Event Trigger and the Deadband submodule. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Pulse Width Modulator (ePWM) Type 4" (on page 57).

Parameters

System Clock [Hz] (see page 59)
The system clock of the processor defined in Hz.

EPWM Prescaler (see page 59)
Prescaler to divide down the system clock to generate the EPWM clock.

TBCTL (see page 59)
Time-Base control register.

TBCTL2 (see page 60)
Time-Base control register 2.

CMPCTL (see page 63)
Compare control register.

CMPCTL (see page 63)
Compare control register 2.

AQSFRC (see page 64)
Action-Qualifier software force register.

ETSEL (see page 68)
Event-Trigger selection register.

ETPS (see page 68)
Event-Trigger prescale register.

ETCNTINIT (see page 68)
Event-Trigger counter initialization register.

ETSOCPS (see page 68)
Event-Trigger SOC prescale register.

DBCTL (see page 71)
Dead-Band control register.

Initial Counter (see page 60)
Counter initialization.

Initial Direction (see page 60)
Initial direction in up-down-count mode.

Initial State (see page 60)
Initial output state for EPWMA and EPWMB.

Probe Signals

CMPx
Compare register.

AQCTLx
Action qualifier configuration.

AQCTLx2
Action qualifier configuration.

AQCSFRC
Action qualifier software forcing configuration.

EPWMx
EPWM outputs.

EPWMSOCx
EPWM SOC pulse outputs.

TBPRD
Period of PWM counter.

TBCTL
Time-Base control register.

TBCTL2
Time-Base control register 2.

CMPCTL
Compare-Control register.

CMPCTL2
Compare-Control register 2.

AQSFRC
Action-Qualifier software force register.

ETSEL
Event-Trigger selection register.

ETPS
Event-Trigger prescale register.

ETCNTINIT
Event-Trigger counter initialization register.

ETSOCPS
Event-Trigger SOC prescaler register.

DBCTL
Dead-Band control register.

DBRED
Dead-Band generator rising-edge delay register.

DBRED
Dead-Band generator falling-edge delay register.

SYNCI
Synchronization input.

TBPHS
Synchronization value.

SYNCO
Synchronization output.

FLAGS
Counter value, event flags and counting direction.

TI C2000 eQEP Type 0 GUI

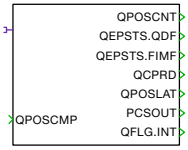
Purpose

High fidelity model of TI's C2000 eQEP module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / eQEP

Description



This block efficiently models the behavior of a TI Type 0 eQEP module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the TI Type 0 eQEP module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Quadrature Encoder Pulse (eQEP) Type 0" (on page 112).

Parameters

ePWM General

System Clock [Hz] (see page 112)
The system clock of the processor defined in Hz.

Quantization Interval (see page 112)
Maps the counter to an integer multiple of the quantization interval: $counter = q * \text{round}\left(\frac{counter}{q}\right)$. The interval refers to the quantum q used in the mapping function.

Quantization Step Detection (see page 112)
When set to `on`, a zero-crossing signal is enabled to help the solver detect the precise instants when the counter increments or decrements by the quantum q. Enabling step detection will influence the solver step size and for fast rotating shafts can severely reduce the simulation speed.

When set to `off`, the quantization will not influence the step size of the solver.

Number of Slots (see page 112)
Number of slots per revolution of the encoder.

Initial Rotor Angle (see page 112)
The mechanical rotor angle θ_{m} in radians.

QEPI Midpoint Offset (see page 112)
Midpoint offset of the QEPI slot in radians.

QEPI Width (see page 112)
Width of the QEPI slot in radians.

QPOSMAX (see page 112)
eQEP Maximum Position Count register.

QPOSINIT (see page 112)
eQEP Position Counter Initialization register.

Low Speed Threshold [rpm] (see page 119)
Speed in rpm above which the unit position subsystem is disabled.

QDECCTL

QDECCTL.SWAP (see page 114)
Swaps the quadrature clock inputs and reverses the counting direction.

QEPCTL

QEPCTL.UTE (see page 119)
Enable unit timer in edge capture unit.

QEPCTL.SWI (see page 116)
Enable initialization of position counter.

QEPCTL.PCRM (see page 116)
Position counter reset mode.

QPOSCTL

QPOSCTL.PCSPW (see page 119)
Position-compare sync output pulse width.

QPOSCTL.PCE (see page 119)
Position-compare enable/disable.

QPOSCTL.PCPOL (see page 119)
Polarity of sync output.

QPOSCTL.PCLOAD (see page 119)
Position-compare shadow load mode.

QEINT

QEINT.QDC (see page 122)
Quadrature direction change interrupt enable.

QEINT.PCU (see page 122)
Position counter underflow interrupt enable.

QEINT.PCO (see page 122)
Position counter overflow interrupt enable.

QEINT.PCM (see page 122)
Position-compare match interrupt enable.

QEINT.UTO (see page 119)
Unit time out interrupt enable.

Edge Capture Unit

QCAPCTL.UPPS (see page 119)
Unit position event prescaler.

QCAPCTL.CCPS (see page 119)
eQEP capture timer clock prescaler.

QCAPCTL.CEN (see page 119)
eQEP capture enable.

QUPRD (see page 119)
Unit timer period register.

Probe Signals

QDECCTL
eQEP decoder control register.

QPOSCMP
eQEP position-compare register.

QEPCTL
eQEP control register.

QPOSCTL
eQEP position-compare control register.

QEINT
eQEP interrupt enable register.

QCAPCTL
eQEP capture control register.

QEPI
QEPI signal.

QEPSTS.COEF
Counter overflow error flag bit in QEPSTS register.

QEPSTS.UPEVENT
Unit position flag bit in QEPSTS register.

QEPSTS.CDEF
Counter direction error flag bit in QEPSTS register.

QUPRD
Unit timer period register.

QUTMR
Unit timer counter register.

QFLG.UTO
Unit time out event flag.

Unit Position Enabled/Disabled
Flag indicating if the unit position module is enabled or disabled. If the speed of the encoder is greater than the Low Speed Threshold the unit position module is disabled.

TI C2000 eQEP Type 0 REG

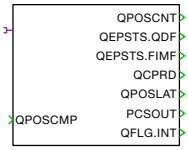
Purpose

High fidelity model of TI's C2000 eQEP module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / TI C2000 / eQEP

Description



This block efficiently models the behavior of a TI Type 0 eQEP module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation "Enhance Quadrature Encoder Pulse (eQEP) Type 0" (on page 112).

Parameters

System Clock [Hz] (see page 112)
The system clock of the processor defined in Hz.

Quantization Interval (see page 112)
Maps the counter to an integer multiple of the quantization interval: $counter = q * \text{round}\left(\frac{counter}{q}\right)$. The interval refers to the quantum q used in the mapping function.

Quantization Step Detection (see page 112)
When set to `on`, a zero-crossing signal is enabled to help the solver detect the precise instants when the counter increments or decrements by the quantum q. Enabling step detection will influence the solver step size and for fast rotating shafts can severely reduce the simulation speed.

When set to `off`, the quantization will not influence the step size of the solver.

Number of Slots (see page 112)
Number of slots per revolution of the encoder.

Initial Rotor Angle (see page 112)
The mechanical rotor angle θ_{m} in radians.

QEPI Midpoint Offset (see page 112)
Midpoint offset of the QEPI slot in radians.

QEPI Width (see page 112)
Width of the QEPI slot in radians.

QPOSMAX (see page 112)
eQEP Maximum Position Count register.

QPOSINIT (see page 112)
eQEP Position Counter Initialization register.

QDECCTL (see page 114)
eQEP decoder control register.

QEPCTL (see page 116)
eQEP control register.

QPOSCTL (see page 119)
eQEP position-compare control register.

QEINT (see page 122)
eQEP interrupt enable register.

QCAPCTL (see page 119)
eQEP capture control register.

QUPRD (see page 119)
Unit timer period register.

Low Speed Threshold [rpm] (see page 119)
Speed in rpm above which the unit position subsystem is disabled.

Probe Signals

QDECCTL
eQEP decoder control register.

QPOSCMP
eQEP position-compare register.

QEPCTL
eQEP control register.

QPOSCTL
eQEP position-compare control register.

QEINT
eQEP interrupt enable register.

QCAPCTL
eQEP capture control register.

QEPI
QEPI signal.

QEPSTS.COEF
Counter overflow error flag bit in QEPSTS register.

QEPSTS.UPEVENT
Unit position flag bit in QEPSTS register.

QEPSTS.CDEF
Counter direction error flag bit in QEPSTS register.

QUPRD
Unit timer period register.

QUTMR
Unit timer counter register.

QFLG.UTO
Unit time out event flag.

Unit Position Enabled/Disabled
Flag indicating if the unit position module is enabled or disabled. If the speed of the encoder is greater than the Low Speed Threshold the unit position module is disabled.

STM32 F0 ADC GUI

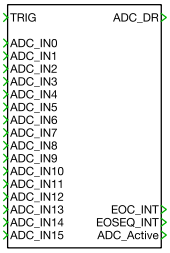
Purpose

High fidelity model of STM32 F0 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F0 / ADC

Description



This block models the STM F0 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM F0 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 148).

Parameters

ADC General

PCLK [Hz] (see page 150)
The clock potentially used as as the adc time base in Hz.

ADC_CFGR2.CKMODE [Hz] (see page 150)
Determines the adc time base.

Reference[LO,HI] (see page 150)
Specification of the reference voltage in mask.

ADC_CFGR1.DISCEN (see page 152)
Enables/disables discontinuous mode for regular channels.

ADC_CFGR1.RES (see page 150)
Defines ADC resolution.

Output Mode (see page 150)
Defines representation of conversion results.

ADC_SMPR.SMP (see page 152)
Defines adc sample window.

ADC_IER.EOCIE (see page 155)
Enables/disables interrupt pulses on EOC_INT.

ADC_IER.EOSEQIE (see page 155)
Enables/disables interrupt pulses on EOSEQ_INT.

Minimum Trigger Latency (see page 154)
Defines the latency between a trigger and start of the sampling window.

Register Write Latency (see page 154)
Defines the latency between EOC and latch into the register.

ADC Channel Selection

ADC_CHSELR.CHSELx (see page 152)
Defines channel x to be an element of the conversion sequence.

Probe Signals

ADC_CFGR1
ADC Control register resulting from mask settings.

ADC_CFGR2
ADC Control register resulting from mask settings.

ADC_SMPR
Sample time control register resulting from mask settings.

ADC_IER
Interrupt enable register resulting from mask settings.

ADC_CHSELR
Channel selection register resulting from mask settings.

STM32 F0 ADC REG

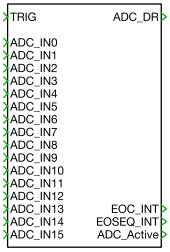
Purpose

High fidelity model of STM32 F0 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F0 / ADC

Description



This block models the STM32 F0 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 148).

Parameters

PCLK [Hz] (see page 150)
The clock potentially used as as the adc time base in Hz.

ADC_CFGR1 (see page 152)
ADC Configuration register 1.

ADC_CFGR2 (see page 152)
ADC Configuration register 2.

ADC_SMPR (see page 152)
ADC sample time control register.

ADC_IER (see page 155)
ADC interrupt enable register.

ADC_CHSELR (see page 152)
ADC channel selection register.

Reference[LO,HI] (see page 150)
Specification of the reference voltage in mask.

Output Mode (see page 150)
Defines representation of conversion results.

Minimum Trigger Latency (see page 154)
Defines the latency between a trigger and start of the sampling window.

Register Write Latency (see page 154)
Defines the latency between EOC and latch into the register.

Probe Signals

ADC_CFGR1
ADC Control register resulting from mask settings.

ADC_CFGR2
ADC Control register resulting from mask settings.

ADC_SMPR
Sample time control register resulting from mask settings.

ADC_IER
Interrupt enable register resulting from mask settings.

ADC_CHSELR
Channel selection register resulting from mask settings.

STM32 F0 Timer Output Configurator

Purpose

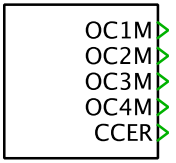
Helper block for generation of OCxM and CCER registers.

Library

Processor in the Loop / Peripherals / STM32 F0 / Timer

Description

This block generates the decimal value for the Output Compare mode register cells (OCxM) and the Capture Compare Enable register (CCER) based on the configuration of the mask parameters.



Parameters

Output Compare Mode

Register cells for configuration of output channels 1-4

OC1M
Output Compare mode for output channel 1.

OC2M
Output Compare mode for output channel 2.

OC3M
Output Compare mode for output channel 3.

OC4M
Output Compare mode for output channel 4.

Compare Enable Register

Control of output stage and signal polarity

CCxE
Activates output enable circuit for channel x.

CCxNE
Activates output enable circuit for complementary channel x.

CCxP
Controls polarity of channel x.

CCxNP
Controls polarity of complementary channel x.

STM32 F0 Timer Output GUI

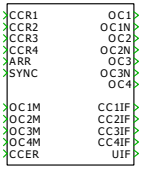
Purpose

High fidelity model of the STM32 F0 module with focus on output behavior and Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F0 / Timer

Description



This block efficiently models the behavior of a STM32 F0 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM32 F0 timer module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 127).

Parameters

TIM General

Timer Type (see page 128)
Specifies used timer subtype.

CK_PSC [Hz] (see page 128)
Counter clock frequency defined in Hz.

TIM_PSC (see page 128)
A prescaler for the counter time base calculation.

TIM_CR1.CKD (see page 134)
Determines t_{dts} used for dead-time calculation.

TIM_CR1.CMS (see page 128)
Defines counter mode.

TIM_CR1.DIR (see page 128)
Defines counter direction in Edge-aligned mode.

TIM_BDTR.DTG (see page 134)
Configures dead-time for advanced and complementary timer subtypes.

Initial Counter (see page 131)
Counter initialization.

Initial Direction (see page 131)
Initial counter direction in Center-aligned mode.

TIM INT Enable

Enables Interrupt flag generation on CCxIF and UIF terminals.

TIM_DIER.CCxIE (see page 131)
Enables pulse on CCxIF terminal.

TIM_DIER.UIE (see page 131)
Enables pulse on UIF terminal.

GPIO Mode

Configuration of output level if output enable circuit is inactive.

GPIOM.OCx (see page 147)
Inactive level for channel x.

GPIOM.OCxN (see page 147)
Inactive level for complementary channel x.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F0 Timer Output REG

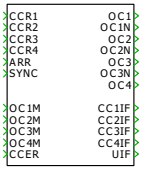
Purpose

High fidelity model of the STM32 F0 module with focus on output behavior and register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F0 / Timer

Description



This block efficiently models the behavior of a STM32 F0 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 127).

Parameters

Timer Type (see page 128)
Specifies used timer subtype.

CK_PSC [Hz] (see page 128)
Counter clock frequency defined in Hz.

TIM_PSC (see page 128)
A prescaler for the counter time base calculation.

TIM_CR1 (see page 128)
Timer control register 1.

TIM_BDTR (see page 134)
Timer dead-time register.

TIM_DIER (see page 131)
Timer interrupt enable register.

GPIO Mode (see page 147)
GPIO Mode configuration register.

Initial Counter (see page 131)
Counter initialization.

Initial Direction (see page 131)
Initial counter direction in Center-aligned mode.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F1 ADC GUI

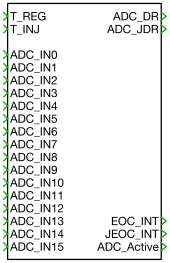
Purpose

High fidelity model of STM32 F1 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F1 / ADC

Description



This block models the STM F1 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM F1 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 182).

Parameters

ADC General

ADC_CLK [Hz] (see page 184)
The clock used as as the adc time base in Hz.

Reference[LO,HI] (see page 184)
Specification of the reference voltage in mask.

ADC_CR1.DISCNUM (see page 184)
Defines regular channels converted in discontinuous mode.

ADC_CR1.JDISCEN (see page 184)
Enables discontinuous mode for injected channels.

ADC_CR1.DISCEN (see page 184)
Enables/disables discontinuous mode for regular channels.

ADC_CR1.JAUTO (see page 184)
Enables/disables automatic injected group conversion.

ADC_CR1.SCAN (see page 184)
Enables/disables scan mode.

ADC_CR1.JEOCIE (see page 188)
Enables/disables interrupt pulses on JEOC_INT.

ADC_CR1.EOCIE (see page 188)
Enables/disables interrupt pulses on EOC_INT.

Output Mode (see page 184)
Defines representation of conversion results.

ADC_SMPRx

ADC_SMPRx.SMPy (see page 184)
Defines sampling length for corresponding input.

ADC_SQRx

ADC_SQRx.L (see page 184)
Defines regular group length and dimension of ADC_DR.

ADC_SQRx.SQy (see page 184)
Defines input sampled by regular group element y.

ADC_JSQR

ADC_SQR.JL (see page 184)
Defines injected group length and dimension of ADC_JDR.

ADC_JSQR.JSQy (see page 184)
Defines input sampled by injected group element y.

Probe Signals

ADC_CR1
ADC Control register resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F1 ADC REG

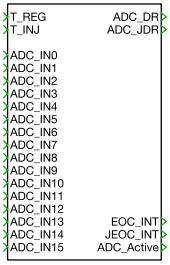
Purpose

High fidelity model of STM32 F1 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F1 / ADC

Description



This block models the STM32 F1 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 182).

Parameters

ADC_CLK [Hz] (see page 184)
The clock used as as the adc time base in Hz.

Reference[LO,HI] (see page 184)
Specification of the reference voltage in mask.

ADC_CR1 (see page 184)
ADC Control register 1.

ADC_SMPRx (see page 184)
ADC sample time control registers.

ADC_SQRx (see page 184)
ADC regular sequence control registers.

ADC_JSQR (see page 184)
ADC injected sequence control register.

Output Mode (see page 184)
Defines representation of conversion results.

Probe Signals

ADC_CR1
ADC Control register resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F1 Timer Output Configurator

Purpose

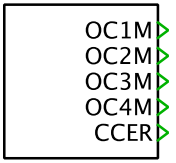
Helper block for generation of OCxM and CCER registers.

Library

Processor in the Loop / Peripherals / STM32 F1 / Timer

Description

This block generates the decimal value for the Output Compare mode register cells (OCxM) and the Capture Compare Enable register (CCER) based on the configuration of the mask parameters.



Parameters

Output Compare Mode

Register cells for configuration of output channels 1-4

OC1M
Output Compare mode for output channel 1.

OC2M
Output Compare mode for output channel 2.

OC3M
Output Compare mode for output channel 3.

OC4M
Output Compare mode for output channel 4.

Compare Enable Register

Control of output stage and signal polarity

CCxE
Activates output enable circuit for channel x.

CCxNE
Activates output enable circuit for complementary channel x.

CCxP
Controls polarity of channel x.

CCxNP
Controls polarity of complementary channel x.

STM32 F1 Timer Output GUI

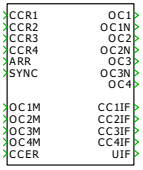
Purpose

High fidelity model of the STM32 F1 module with focus on output behavior and Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F1 / Timer

Description



This block efficiently models the behavior of a STM32 F1 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM32 F1 timer module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 159).

Parameters

TIM General

Timer Type (see page 160)
Specifies used timer subtype.

CK_PSC [Hz] (see page 160)
Counter clock frequency defined in Hz.

TIM_PSC (see page 160)
A prescaler for the counter time base calculation.

TIM_CR1.CKD (see page 166)
Determines t_{dts} used for dead-time calculation.

TIM_CR1.CMS (see page 160)
Defines counter mode.

TIM_CR1.DIR (see page 160)
Defines counter direction in Edge-aligned mode.

TIM_BDTR.DTG (see page 166)
Configures dead-time for advanced and complementary timer subtypes.

Initial Counter (see page 163)
Counter initialization.

Initial Direction (see page 163)
Initial counter direction in Center-aligned mode.

TIM INT Enable

Enables Interrupt flag generation on CCxIF and UIF terminals.

TIM_DIER.CCxIE (see page 163)
Enables pulse on CCxIF terminal.

TIM_DIER.UIE (see page 163)
Enables pulse on UIF terminal.

GPIO Mode

Configuration of output level if output enable circuit is inactive.

GPIOM.OCx (see page 181)
Inactive level for channel x.

GPIOM.OCxN (see page 181)
Inactive level for complementary channel x.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F1 Timer Output REG

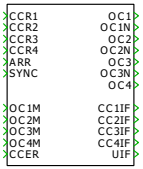
Purpose

High fidelity model of the STM32 F1 module with focus on output behavior and register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F1 / Timer

Description



This block efficiently models the behavior of a STM32 F1 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 159).

Parameters

Timer Type (see page 160)
Specifies used timer subtype.

CK_PSC [Hz] (see page 160)
Counter clock frequency defined in Hz.

TIM_PSC (see page 160)
A prescaler for the counter time base calculation.

TIM_CR1 (see page 160)
Timer control register 1.

TIM_BDTR (see page 166)
Timer dead-time register.

TIM_DIER (see page 163)
Timer interrupt enable register.

GPIO Mode (see page 181)
GPIO Mode configuration register.

Initial Counter (see page 163)
Counter initialization.

Initial Direction (see page 163)
Initial counter direction in Center-aligned mode.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F3 ADC GUI

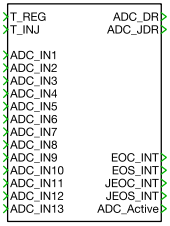
Purpose

High fidelity model of STM32 F3 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F3 / ADC

Description



This block models the STM F3 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM F3 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 211).

Parameters

ADC General

ADC_CLK [Hz] (see page 213)
The clock used as the adc time base in Hz.

Reference[LO,HI] (see page 213)
Specification of the reference voltage in mask.

ADC_CFGR.JAUTO (see page 215)
Enables/disables automatic injected group conversion.

ADC_CFGR.JDISCEN (see page 215)
Enables discontinuous mode for injected channels.

ADC_CFGR.DISCNUM (see page 215)
Defines regular channels converted in discontinuous mode.

ADC_CFGR.DISCEN (see page 215)
Enables/disables discontinuous mode for regular channels.

ADC_CFGR.RES (see page 213)
Defines ADC resolution.

ADC_IER.JEOSIE (see page 220)
Enables/disables interrupt pulses on JEOS_INT.

ADC_IER.JEOCIE (see page 220)
Enables/disables interrupt pulses on JEOC_INT.

ADC_IER.EOSIE (see page 220)
Enables/disables interrupt pulses on EOS_INT.

ADC_IER.EOCIE (see page 220)
Enables/disables interrupt pulses on EOC_INT.

Output Mode (see page 213)
Defines representation of conversion results.

ADC_DIFSEL

ADC_DIFSELx (see page 215)
Defines conversion mode for corresponding input.

ADC_SMPRx

ADC_SMPRx.SMPy (see page 215)
Defines sampling length for corresponding input.

ADC_SQRx

ADC_SQRx.L (see page 215)
Defines regular group length and dimension of ADC_DR.

ADC_SQRx.SQy (see page 215)
Defines input sampled by regular group element y.

ADC_JSQR

ADC_SQR.JL (see page 215)
Defines injected group length and dimension of ADC_JDR.

ADC_JSQR.JSQy (see page 215)
Defines input sampled by injected group element y.

Probe Signals

ADC_CFGR
ADC control register resulting from mask settings.

ADC_DIFSEL
ADC mode selection register resulting from mask settings.

ADC_IER
ADC interrupt settings register resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F3 ADC REG

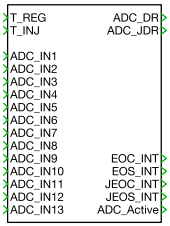
Purpose

High fidelity model of STM32 F3 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F3 / ADC

Description



This block models the STM32 F3 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 211).

Parameters

ADC_CLK [Hz] (see page 213)
The clock used as the adc time base in Hz.

Reference[LO,HI] (see page 213)
Specification of the reference voltage in mask.

ADC_CFGR (see page 215)
ADC control register.

ADC_DIFSEL (see page 215)
ADC mode selection register.

ADC_IER (see page 215)
ADC interrupt settings register.

ADC_SMPRx (see page 215)
ADC sample time control registers.

ADC_SQRx (see page 215)
ADC regular sequence control registers.

ADC_JSQR (see page 215)
ADC injected sequence control register.

Output Mode (see page 213)
Defines representation of conversion results.

Probe Signals

ADC_CFGR
ADC control register resulting from mask settings.

ADC_DIFSEL
ADC mode selection register resulting from mask settings.

ADC_IER
ADC interrupt settings register resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F3 Timer Output Configurator

Purpose

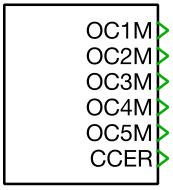
Helper block for generation of OCxM and CCER registers.

Library

Processor in the Loop / Peripherals / STM32 F3 / Timer

Description

This block generates the decimal value for the Output Compare mode register cells (OCxM) and the Capture Compare Enable register (CCER) based on the configuration of the mask parameters.



Parameters

Output Compare Mode

Register cells for configuration of output channels 1-5

OC1M
Output Compare mode for output channel 1.

OC2M
Output Compare mode for output channel 2.

OC3M
Output Compare mode for output channel 3.

OC4M
Output Compare mode for output channel 4.

OC5M
Output Compare mode for output channel 5.

Compare Enable Register

Control of output stage and signal polarity

CCxE
Activates output enable circuit for channel x.

CCxNE
Activates output enable circuit for complementary channel x.

CCxP
Controls polarity of channel x.

CCxNP
Controls polarity of complementary channel x.

STM32 F3 Timer Output GUI

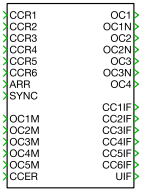
Purpose

High fidelity model of the STM32 F3 module with focus on output behavior and Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F3 / Timer

Description



This block efficiently models the behavior of a STM32 F3 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM32 F3 timer module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 193).

Parameters

TIM General

Timer Type (see page 194)
Specifies used timer subtype.

CK_PSC [Hz] (see page 194)
Counter clock frequency defined in Hz.

TIM_PSC (see page 194)
A prescaler for the counter time base calculation.

TIM_CR1.CKD (see page 200)
Determines t_{dts} used for dead-time calculation.

TIM_CR1.CMS (see page 194)
Defines counter mode.

TIM_CR1.DIR (see page 194)
Defines counter direction in Edge-aligned mode.

TIM_BDTR.DTG (see page 200)
Configures dead-time for advanced timer subtype.

Initial Counter (see page 197)
Counter initialization.

Initial Direction (see page 197)
Initial counter direction in Center-aligned mode.

TIM INT Enable

Enables Interrupt flag generation on CCxIF and UIF terminals.

TIM_DIER.CCxIE (see page 197)
Enables pulse on CCxIF terminal.

TIM_DIER.UIE (see page 197)
Enables pulse on UIF terminal.

GPIO Mode

Configuration of output level if output enable circuit is inactive.

GPIOM.OCx (see page 210)
Inactive level for channel x.

GPIOM.OCxN (see page 210)
Inactive level for complementary channel x.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F3 Timer Output REG

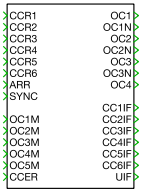
Purpose

High fidelity model of the STM32 F3 module with focus on output behavior and register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F3 / Timer

Description



This block efficiently models the behavior of a STM32 F3 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 193).

Parameters

Timer Type (see page 194)
Specifies used timer subtype.

CK_PSC [Hz] (see page 194)
Counter clock frequency defined in Hz.

TIM_PSC (see page 194)
A prescaler for the counter time base calculation.

TIM_CR1 (see page 194)
Timer control register 1.

TIM_BDTR (see page 200)
Timer dead-time register.

TIM_DIER (see page 197)
Timer interrupt enable register.

GPIO Mode (see page 210)
GPIO Mode configuration register.

Initial Counter (see page 197)
Counter initialization.

Initial Direction (see page 197)
Initial counter direction in Center-aligned mode.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F2/F4 ADC GUI

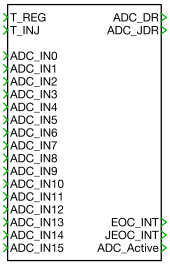
Purpose

High fidelity model of STM32 F2/F4 ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F2/F4 / ADC

Description



This block models the STM F2/F4 ADC module. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM F2/F4 ADC module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 240).

Parameters

ADC General

PCLK2 [Hz] (see page 242)
The clock used as the adc time base in Hz.

ADC_CCR.ADCPRE (see page 242)
Register cell defining a clock prescaler.

Reference[LO,HI] (see page 242)
Specification of the reference voltage in mask.

ADC_CR1.RES (see page 242)
Defines ADC resolution.

ADC_CR1.DISCNUM (see page 243)
Defines regular channels converted in discontinuous mode.

ADC_CR1.JDISCEN (see page 243)
Enables discontinuous mode for injected channels.

ADC_CR1.DISCEN (see page 243)
Enables/disables discontinuous mode for regular channels.

ADC_CR1.JAUTO (see page 243)
Enables/disables automatic injected group conversion.

ADC_CR1.SCAN (see page 243)
Enables/disables scan mode.

ADC_CR1.JEOCIE (see page 248)
Enables/disables interrupt pulses on JEOC_INT.

ADC_CR1.EOCIE (see page 248)
Enables/disables interrupt pulses on EOC_INT.

ADC_CR2.EOCS (see page 243)
Defines EOC flag occurrence in scan mode.

Output Mode (see page 242)
Defines representation of conversion results.

ADC_SMPRx

ADC_SMPRx.SMPy (see page 243)
Defines sampling length for corresponding input.

ADC_SQRx

ADC_SQRx.L (see page 243)
Defines regular group length and dimension of ADC_DR.

ADC_SQRx.SQy (see page 243)
Defines input sampled by regular group element y.

ADC_JSQR

ADC_SQR.JL (see page 243)
Defines injected group length and dimension of ADC_JDR.

ADC_JSQR.JSQy (see page 243)
Defines input sampled by injected group element y.

Probe Signals

ADC_CCR
ADC Common Control register resulting from mask settings.

ADC_CRx
ADC Control registers resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F2/F4 ADC REG

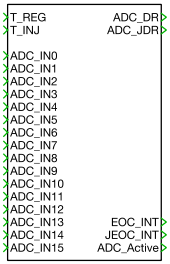
Purpose

High fidelity model of STM32 F2/F4 ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F2/F4 / ADC

Description



This block models the STM32 F2/F4 ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Analog Digital Converter (ADC)” (on page 240).

Parameters

PCLK2 [Hz] (see page 242)
The clock used as as the adc time base in Hz.

ADC_CCR (see page 242)
Common control register defining a clock prescaling.

Reference[LO,HI] (see page 242)
Specification of the reference voltage in mask.

ADC_CR1 (see page 243)
ADC Control register 1.

ADC_CR2 (see page 243)
ADC Control register 2.

ADC_SMPRx (see page 243)
ADC sample time control registers.

ADC_SQRx (see page 243)
ADC regular sequence control registers.

ADC_JSQR (see page 243)
ADC injected sequence control register.

Output Mode (see page 242)
Defines representation of conversion results.

Probe Signals

ADC_CCR
ADC Common Control register resulting from mask settings.

ADC_CRx
ADC Control registers resulting from mask settings.

ADC_SMPRx
Sample time control registers resulting from mask settings.

ADC_SQRx
Regular sequence registers resulting from mask settings.

ADC_JSQR
Injected sequence register resulting from mask settings.

STM32 F2/F4 Timer Output Configurator

Purpose

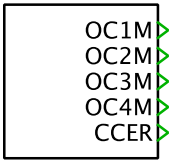
Helper block for generation of OCxM and CCER registers.

Library

Processor in the Loop / Peripherals / STM32 F2/F4 / Timer

Description

This block generates the decimal value for the Output Compare mode register cells (OCxM) and the Capture Compare Enable register (CCER) based on the configuration of the mask parameters.



Parameters

Output Compare Mode

Register cells for configuration of output channels 1-4

OC1M
Output Compare mode for output channel 1.

OC2M
Output Compare mode for output channel 2.

OC3M
Output Compare mode for output channel 3.

OC4M
Output Compare mode for output channel 4.

Compare Enable Register

Control of output stage and signal polarity

CCxE
Activates output enable circuit for channel x.

CCxNE
Activates output enable circuit for complementary channel x.

CCxP
Controls polarity of channel x.

CCxNP
Controls polarity of complementary channel x.

STM32 F2/F4 Timer Output GUI

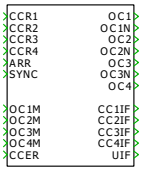
Purpose

High fidelity model of the STM32 F2/F4 module with focus on output behavior and Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / STM32 F2/F4 / Timer

Description



This block efficiently models the behavior of a STM32 F2/F4 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the STM32 F2/F4 timer module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 225).

Parameters

TIM General

Timer Type (see page 226)
Specifies used timer subtype.

CK_PSC [Hz] (see page 226)
Counter clock frequency defined in Hz.

TIM_PSC (see page 226)
A prescaler for the counter time base calculation.

TIM_CR1.CKD (see page 232)
Determines t_{dts} used for dead-time calculation.

TIM_CR1.CMS (see page 226)
Defines counter mode.

TIM_CR1.DIR (see page 226)
Defines counter direction in Edge-aligned mode.

TIM_BDTR.DTG (see page 232)
Configures dead-time for advanced timer subtype.

Initial Counter (see page 229)
Counter initialization.

Initial Direction (see page 229)
Initial counter direction in Center-aligned mode.

TIM INT Enable

Enables Interrupt flag generation on CCxIF and UIF terminals.

TIM_DIER.CCxIE (see page 229)
Enables pulse on CCxIF terminal.

TIM_DIER.UIE (see page 229)
Enables pulse on UIF terminal.

GPIO Mode

Configuration of output level if output enable circuit is inactive.

GPIOM.OCx (see page 239)
Inactive level for channel x.

GPIOM.OCxN (see page 239)
Inactive level for complementary channel x.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

STM32 F2/F4 Timer Output REG

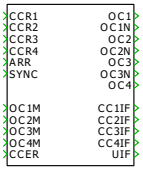
Purpose

High fidelity model of the STM32 F2/F4 module with focus on output behavior and register based configuration.

Library

Processor in the Loop / Peripherals / STM32 F2/F4 / Timer

Description



This block efficiently models the behavior of a STM32 F2/F4 timer module with full timing resolution for a variable PWM period. This component is focussed on PWM generation and therefore on the compare/output features of the timer. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “System Timer for PWM generation (Output Mode)” (on page 225).

Parameters

Timer Type (see page 226)
Specifies used timer subtype.

CK_PSC [Hz] (see page 226)
Counter clock frequency defined in Hz.

TIM_PSC (see page 226)
A prescaler for the counter time base calculation.

TIM_CR1 (see page 226)
Timer control register 1.

TIM_BDTR (see page 232)
Timer dead-time register.

TIM_DIER (see page 229)
Timer interrupt enable register.

GPIO Mode (see page 239)
GPIO Mode configuration register.

Initial Counter (see page 229)
Counter initialization.

Initial Direction (see page 229)
Initial counter direction in Center-aligned mode.

Probe Signals

CCRx
Compare register.

OCxM
Output compare mode.

CCER
Timer Compare enable register.

OCx
Output channels.

OCxN
Complementary output channels.

CCxIF
Compare interrupt flags.

UIF
Update event interrupt flags.

TIM_ARR
Timer auto-reload register.

TIM_CR1
Timer control register 1.

TIM_PSC
Timer prescaler register.

TIM_DIER
Timer interrupt enable register.

TIM_BDTR
Timer dead-time register.

FLAGS
Counter value, event flags and counter direction.

MC dsPIC33F MCADC GUI

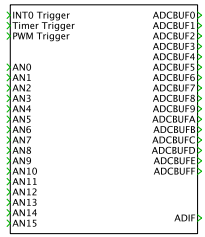
Purpose

High fidelity model of the Microchip dsPIC33F motor control ADC module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / ADC

Description



This block efficiently models the behavior of a Microchip dsPIC33F motor control PWM module with full timing resolution for a variable PWM period. The module is configured using a graphical user interface. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the Microchip motor control module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Microchip Motor Control ADC” (on page 264).

Parameters

ADC General

System clock [Hz] (see page 266)
The system clock of the processor defined in Hz.

Internal RC clock [Hz] (see page 266)
PWM time base control register.

External Reference [Vref-, Vref+] (see page 266)
Specification of external reference voltage in mask.

Internal Reference [AVSS,AVDD] (see page 266)
Specification of internal reference voltage in mask.

Output Mode (see page 266)
Defines representation of conversion results.

ADC Control Register

ADCON1.SIMSAM (see page 269)
Select multi-channel sequential or simultaneous sampling mode.

ADCON1.SSRC (see page 268)
Select ADC start-of-conversion trigger.

ADCON1.FORM (see page 266)
Select output data format.

ADCON1.AD12B (see page 266)
Select ADC resolution.

ADCON2.ALTS (see page 271)
Select fixed or alternative sampling mode.

ADCON2.BUFM (see page 274)
Select buffer fill mode.

ADCON2.SMPI (see page 273)
Select the sample and conversion operation bits value.

ADCON2.CHPS (see page 266)
Select channels to be converted.

ADCON2.CSCNA (see page 271)
Enable channel 0 scan mode operation.

ADCON2.VCFG (see page 266)
Select ADC reference voltage.

ADCON3.ADCS (see page 266)
A prescaler for the ADC time base calculation.

ADCON3.ADRC (see page 266)
Select ADC clock source.

ADC Channel Select

ADCHS123.CH123SA (see page 271)
Select analog input channels as the positive input for MUXA.

ADCHS123.CH123NA (see page 271)
Select analog input channel or voltage reference as the negative input for MUXA.

ADCHS123.CH123SB (see page 271)
Select analog input channels as the positive input for MUXB.

ADCHS123.CH123NB (see page 271)
Select analog input channel or voltage reference as the negative input for MUXB.

ADCHS0.CH0SA (see page 271)
Select analog input channels as the positive input for MUXA.

ADCHS0.CH0NA (see page 271)
Select analog input channel or voltage reference as the negative input for MUXA.

ADCHS0.CH0SB (see page 271)
Select analog input channels as the positive input for MUXB.

ADCHS0.CH0NB (see page 271)
Select analog input channel or voltage reference as the negative input for MUXB.

ADC Channel Scan

CSSx (see page 271)
Enable scan of input ANx when ADC operated in channel scan mode.

Probe Signals

ADCONx
ADC control register x.

ADCHS123
ADC input channel 1, 2, 3 select register.

ADCHS0
ADC input channel 0 select register.

ADCSSL
ADC input scan select register low.

MC dsPIC33F MCADC REG

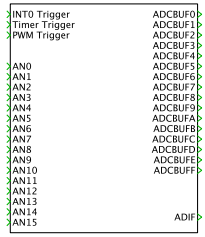
Purpose

High fidelity model of the Microchip dsPIC33F motor control ADC module with register based configuration.

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / ADC

Description



This block models the Microchip motor control ADC module. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Microchip Motor Control ADC” (on page 264).

Parameters

System clock [Hz] (see page 266)
The system clock of the processor defined in Hz.

Internal RC clock [Hz] (see page 266)
PWM time base control register.

External Reference [Vref-, Vref+] (see page 266)
Specification of external reference voltage in mask.

Internal Reference [AVSS,AVDD] (see page 266)
Specification of internal reference voltage in mask.

ADCONx (see page 268)
ADC control register x.

ADCHS123 (see page 271)
ADC input channel 1, 2, 3 select register.

ADCHS0 (see page 271)
ADC input channel 0 select register.

ADCSSL (see page 271)
ADC input scan select register low.

Output Mode (see page 266)
Defines representation of conversion results.

Probe Signals

ADCONx
ADC control register x.

ADCHS123
ADC input channel 1, 2, 3 select register.

ADCHS0
ADC input channel 0 select register.

ADCSSL
ADC input scan select register low.

MC dsPIC33F MCPWM Configurator

Purpose

Helper block for generation of POVDCON register

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / PWM

Description

This block generates the decimal value for the PWM Override Control (POVDCON) register based on the configuration of the mask parameters.

Parameters

POVDCON.POUTxL
PWM manual output bit for low-side PWM pin of module x.

POVDCON.POUTxH
PWM manual output bit for high-side PWM pin of module x.

POVDCON.POVDxL
PWM output override bit for low-side PWM pin of module x.

POVDCON.POVDxH
PWM output override bit for high-side PWM pin of module x.

MC dsPIC33F MCPWM GUI

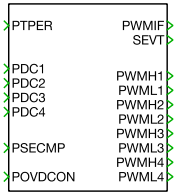
Purpose

High fidelity model of the Microchip dsPIC33F motor control PWM module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / PWM

Description



This block efficiently models the behavior of a Microchip dsPIC33F motor control PWM module with full timing resolution for a variable PWM period. The module is configured using a graphical user interface. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. Under the hood, the resulting register configuration is forwarded to the register based implementation of the Microchip motor control module. The resulting register configuration further is accessible via the probe signals.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Microchip Motor Control PWM” (on page 253).

Parameters

PWM General

Fcy [Hz] (see page 255)
Counter clock frequency defined in Hz.

PTCON.PTMOD (see page 255)
PWM counter mode.

PTCON.PTCKPS (see page 255)
A prescaler for the counter time base calculation.

PTCON.PTOPS (see page 255)
A prescaler for the counter time base calculation.

PWMCON1.PMODx (see page 257)
Specifies operation of PWMx I/O pair in independent or complementary mode.

PWMCON2.OSYNC (see page 258)
Output override synchronization bit.

PWMCON2.SEVOPS (see page 260)
A postscaler for the PWM special event trigger output.

FPOR:POR.HPOL (see page 257)
PWM high-side polarity bit.

FPOR:POR.LPOL (see page 257)
PWM low-side polarity bit.

Dead Time Module

PDTCON1.DTA (see page 261)
Unsigned 6-bit dead time value bits for Dead Time Unit A.

PDTCON1.DTAPS (see page 261)
A prescaler for the PWM Dead Time Unit A.

PDTCON1.DTB (see page 261)
Unsigned 6-bit dead time value bits for Dead Time Unit B.

PDTCON1.DTBPS (see page 261)
A prescaler for the PWM Dead Time Unit B.

PDTCON2.DTSxA (see page 261)
Dead Time Select bits for PWM high-side signal going active for module x.

PDTCON2.DTSxI (see page 261)
Dead Time Select bits for PWM low-side signal going active for module x.

Probe Signals

PTPER
PWM time base period register.

PTCON
PWM time base control register.

PWMCONx
PWM control register x.

PDTCONx
Dead time control register x.

FPOR:POR
Device output pin configuration register.

PWMIF
PWM interrupt flags.

SEVT
PWM Special Event Trigger.

PWMHx
High-side output for PWMx.

PWMLx
Low-side output for PWMx.

PDCx
PWM duty cycle register x.

PSECMP
Special event compare register.

POVDCON
PWM override control register.

MC dsPIC33F MCPWMx GUI

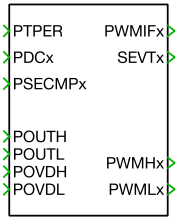
Purpose

High fidelity model of a single Microchip dsPIC33F motor control PWM module with Graphical User Interface configuration.

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / PWM

Description



This block efficiently models the behavior of a single Microchip dsPIC33F motor control PWM module with full timing resolution for a variable PWM period. The module is configured using a graphical user interface. With the Graphical User Interface, the block can simply be configured using combo boxes in the component mask. This is the basic building block that is used in the register based MCPWM implementation which contains 4 modules.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Microchip Motor Control PWM” (on page 253).

Parameters

PWM General

Fcy [Hz] (see page 255)
Counter clock frequency defined in Hz.

PTCON.PTMOD (see page 255)
PWM counter mode.

PTCON.PTCKPS (see page 255)
A prescaler for the counter time base calculation.

PTCON.PTOPS (see page 255)
A prescaler for the counter time base calculation.

PWMCON1.PMOD (see page 257)
Specifies operation of the PWM module I/O pair in independent or complementary mode.

PWMCON2.OSYNC (see page 258)
Output override synchronization bit.

PWMCON2.SEVOPS (see page 260)
A postscaler for the PWM special event trigger output.

FPOR:POR.HPOL (see page 257)
PWM high-side polarity bit.

FPOR:POR.LPOL (see page 257)
PWM low-side polarity bit.

Dead Time Module

PDTCON1.DTA (see page 261)
Unsigned 6-bit dead time value bits for Dead Time Unit A.

PDTCON1.DTAPS (see page 261)
A prescaler for the PWM Dead Time Unit A.

PDTCON1.DTB (see page 261)
Unsigned 6-bit dead time value bits for Dead Time Unit B.

PDTCON1.DTBPS (see page 261)
A prescaler for the PWM Dead Time Unit B.

PDTCON2.DTSA (see page 261)
Dead Time Select bits for PWM high-side signal going active in this module.

PDTCON2.DTSI (see page 261)
Dead Time Select bits for PWM low-side signal going active in this module.

Probe Signals

PTPER
PWM time base period register.

PTCON
PWM time base control register.

PWMCONx
PWM control register x.

PDTCONx
Dead time control register x.

FPOR:POR
Device output pin configuration register.

PWMIF
PWM interrupt flags.

SEVT
PWM Special Event Trigger.

PWMHx
High-side output for PWMx.

PWMLx
Low-side output for PWMx.

PDCx
PWM duty cycle register x.

PSECMP
Special event compare register.

MC dsPIC33F MCPWM REG

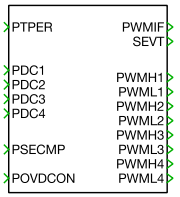
Purpose

High fidelity model of the Microchip dsPIC33F motor control PWM module with register based configuration.

Library

Processor in the Loop / Peripherals / Microchip dsPIC33F / PWM

Description



This block efficiently models the behavior of a Microchip dsPIC33F motor control PWM module with full timing resolution for a variable PWM period. The block is configured using register values which closely emulates the hardware implementation. The registers can be entered in decimal (15), binary (0b1111) or hexadecimal (0xF) representation.

For a detailed description of the supported features and the usage of the block please refer to the detailed documentation “Microchip Motor Control PWM” (on page 253).

Parameters

Fcy [Hz] (see page 255)
Counter clock frequency defined in Hz.

PTCON (see page 255)
PWM time base control register.

PWMCONx (see page 255)
PWM control register x.

PDTCONx (see page 261)
Dead time control register x.

FPOR:POR (see page 257)
Device output pin configuration register.

Probe Signals

PTPER
PWM time base period register.

PTCON
PWM time base control register.

PWMCONx
PWM control register x.

PDTCONx
Dead time control register x.

FPOR:POR
Device output pin configuration register.

PWMIF
PWM interrupt flags.

SEVT
PWM Special Event Trigger.

PWMHx
High-side output for PWMx.

PWMLx
Low-side output for PWMx.

PDCx
PWM duty cycle register x.

PSECMP
Special event compare register.

POVDCON
PWM override control register.

Processor-in-the-Loop

Purpose

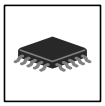
Interface actual code executing on real hardware with simulation

Library

Processor in the Loop

Description

The PLECS PIL block interfaces a plant simulated in PLECS with control code executed on a real micro controller.



For more information on how to work with PIL see section "Processor-in-the-Loop" (on page 5). The PIL block usage and parameters are described in further details in section "PIL Block" (on page 12).

Parameters

General

Target

A PIL block is associated with a target defined in the target manager, which is selected from the Target combo box. The **Configure...** button is a shortcut to the "Target Manager" (on page 9) to configure current and new targets.

Sample time

The PIL block can be triggered at a fixed periodic rate by configuring the sampling time as a positive value. By setting the parameter to **-1** or **[-1 0]** the PIL block will execute with an inherited sample time.

External trigger

The direction of the edges of the trigger signal upon which the PIL block is executed.

Output delay

The delay time between input and output of the PIL block, in seconds. A delay of **0** is a valid setting, but it will create direct-feedthrough between inputs and outputs.

Inputs

Number of inputs (see page 12)

The number of input terminals to the PIL block. Probes can also be added to inputs by selecting them and clicking the **>** button. To remove a probe, select it and either press the **Delete** key or **<** button.

Outputs

Number of outputs (see page 12)
The number of output terminals to the PIL block. Probes can also be added to outputs by selecting them and clicking the **>** button. To remove a probe, select it and either press the **Delete** key or **<** button.

Note It is possible to multiplex several probes into one input/output. The sequence of the probes can be reordered by dragging probes up and down the list.

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plexim

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